

Fig 1

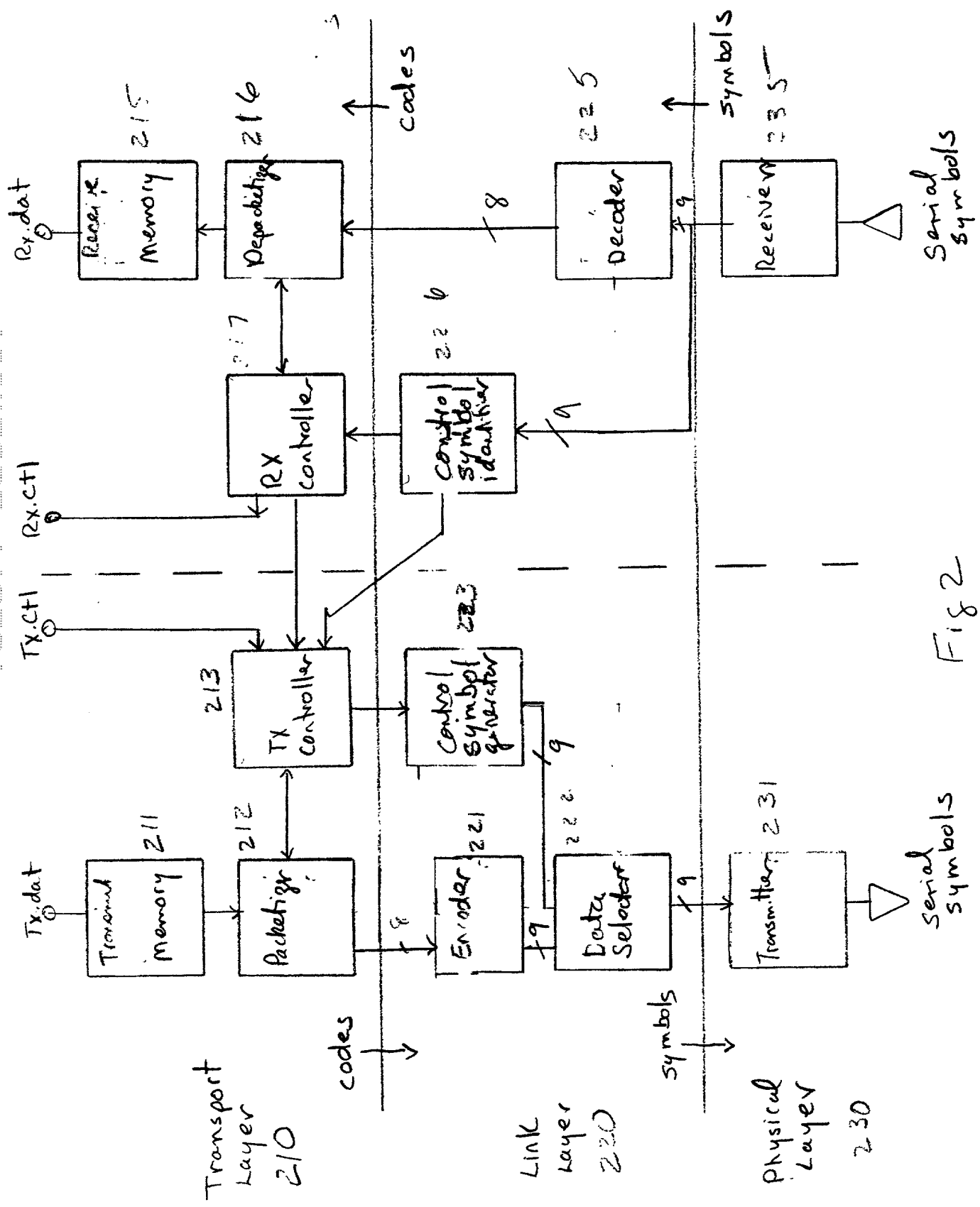


Fig 2

Physical Layer 230

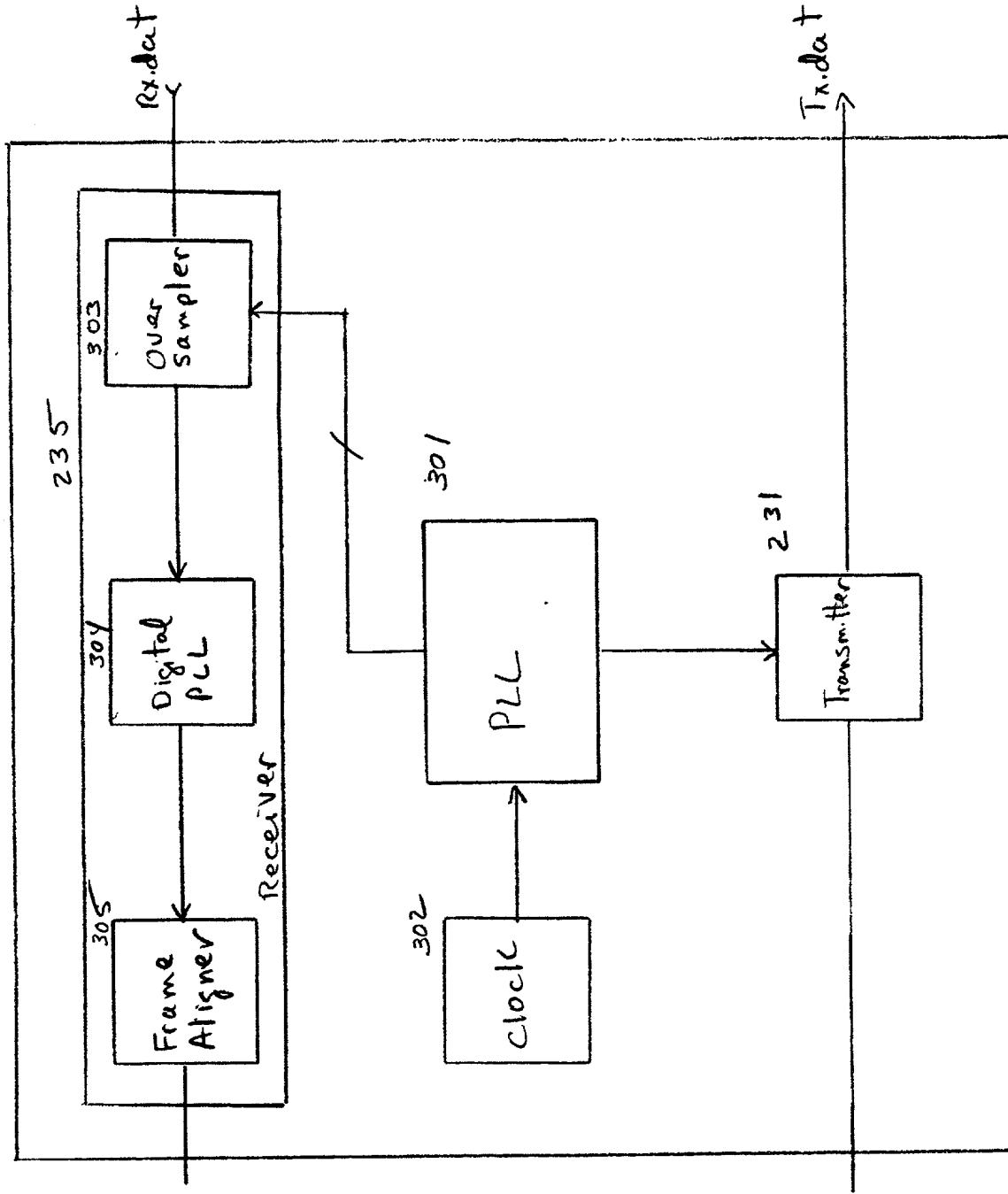


Fig 3

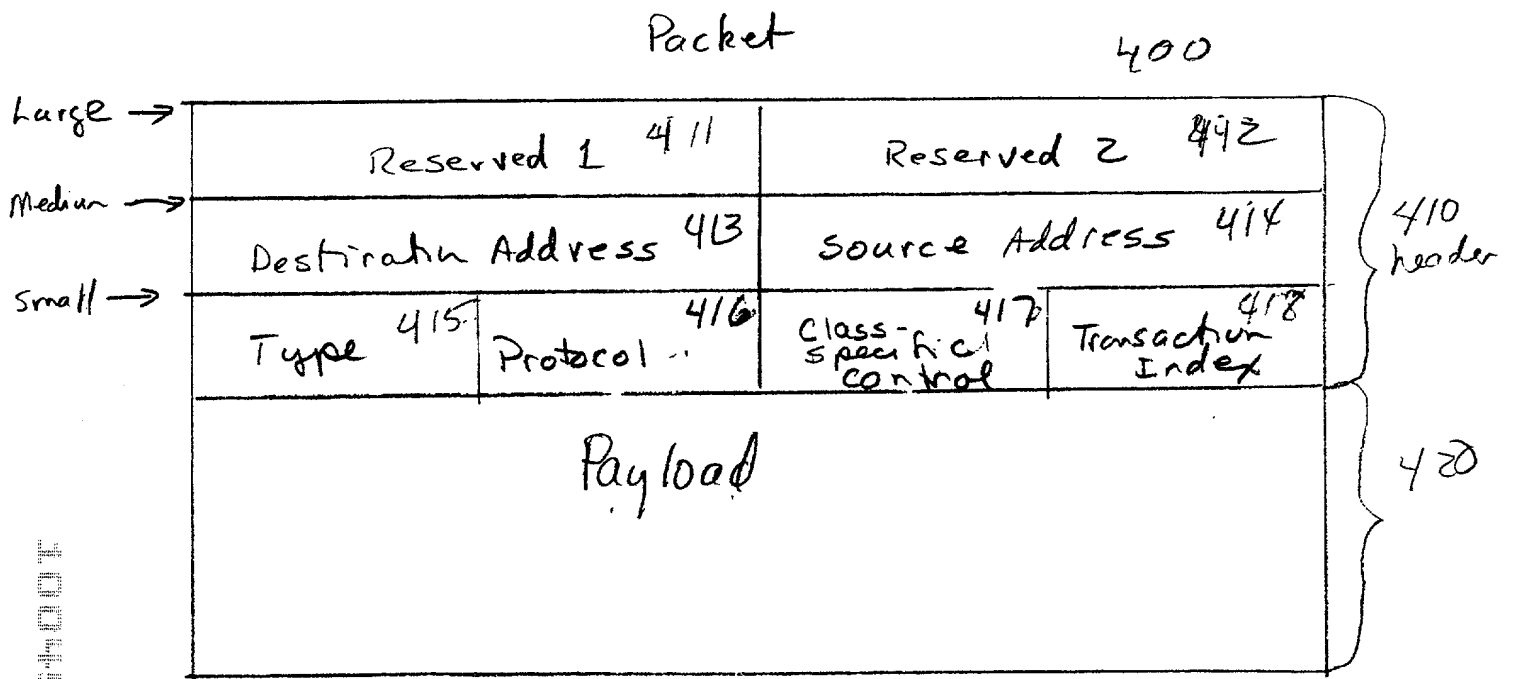
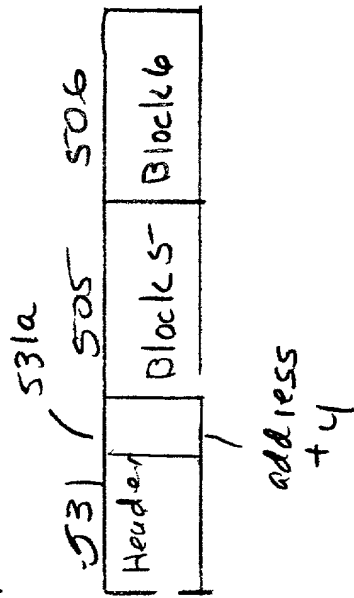
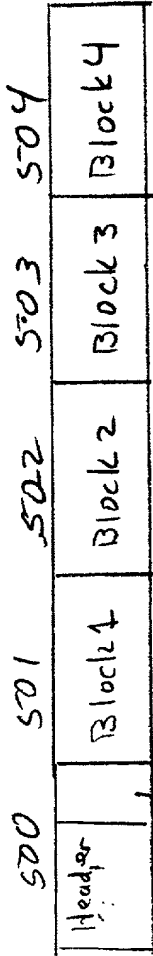
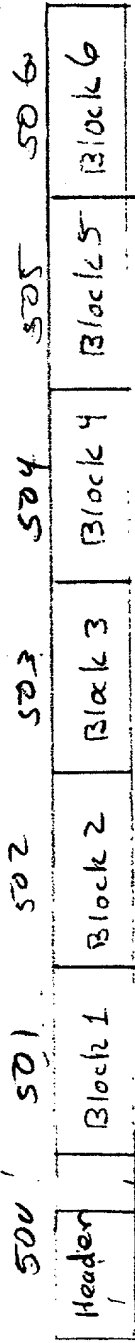


Fig 4

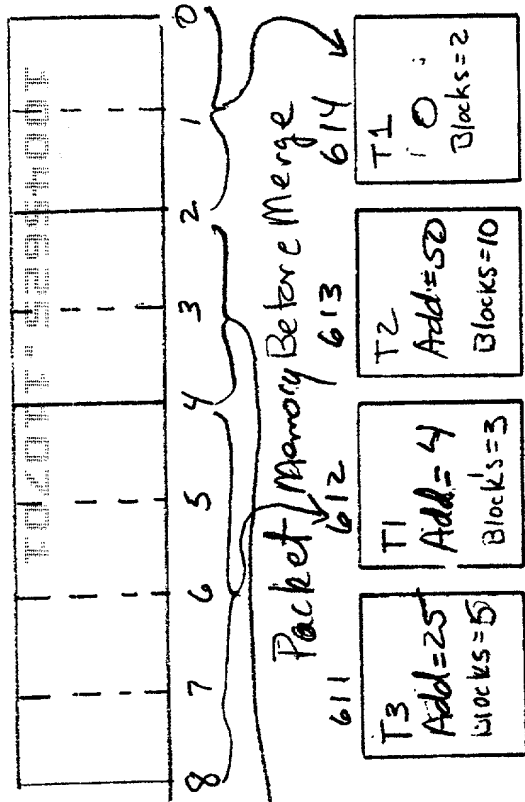
TO Payload Structure



F.45

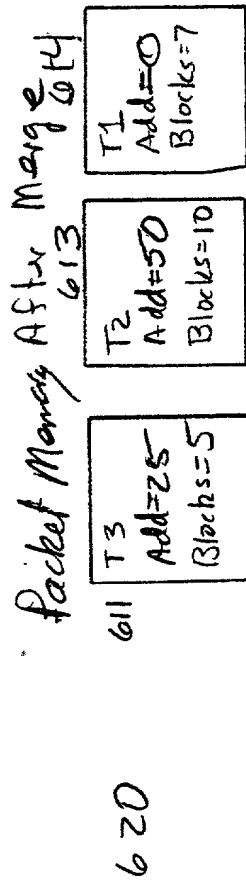
600

T.1



Received Packet
T1 /
Add=2
Blocks=2

630



F. 86

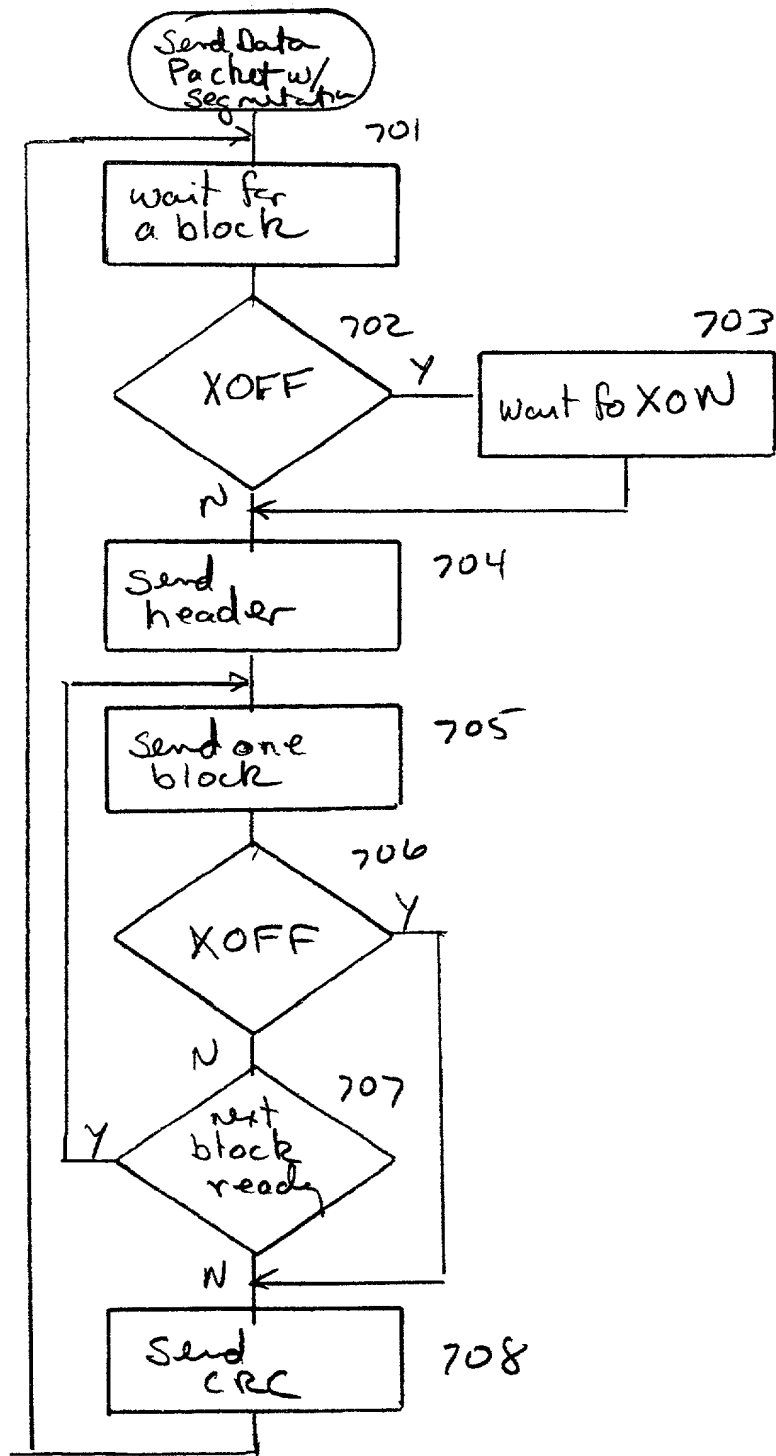


Fig 7

1004563-40701

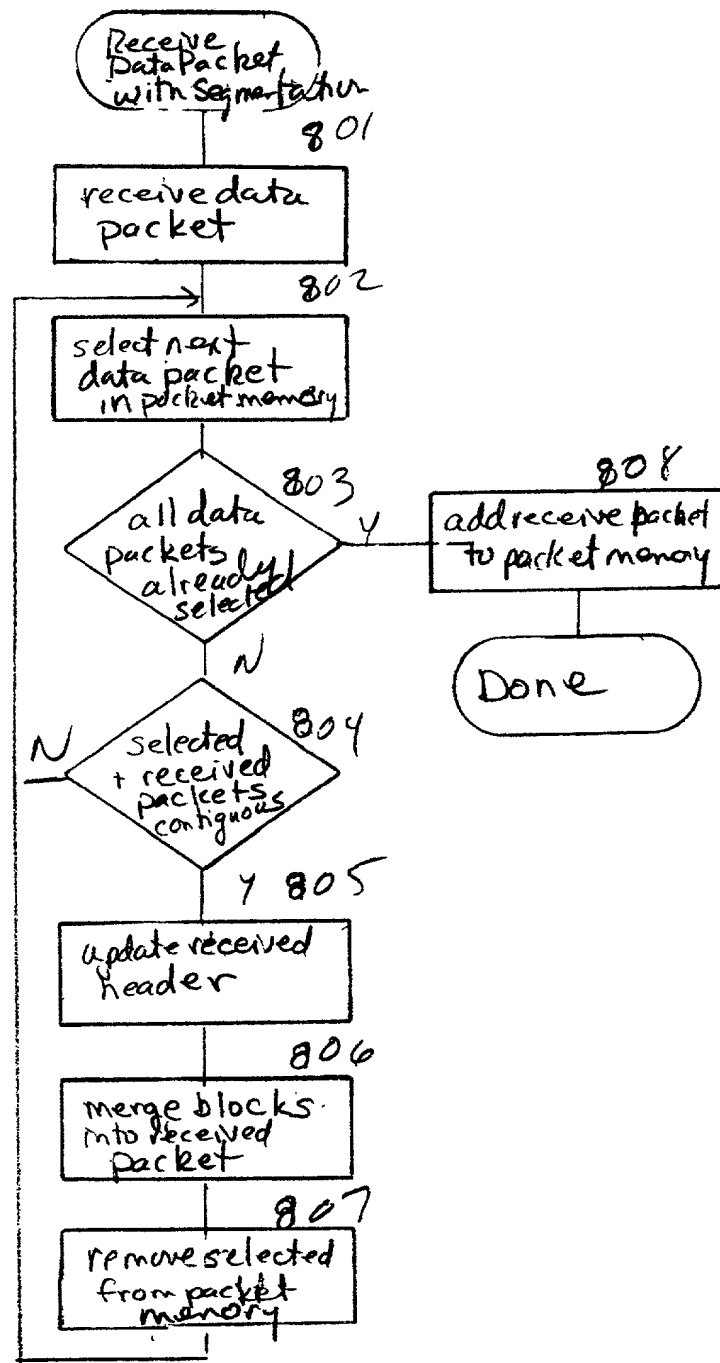
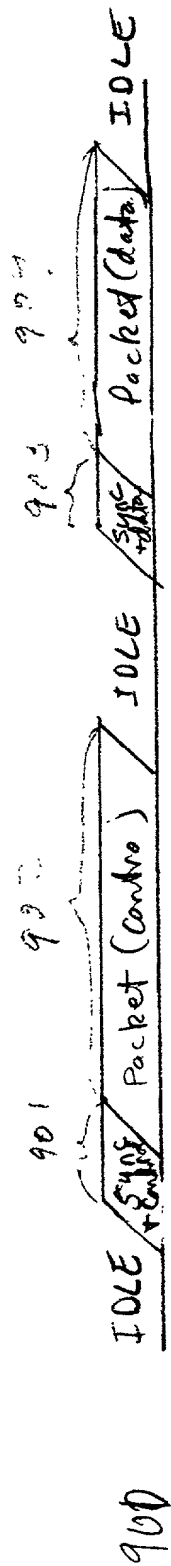


Fig 8



Sync + packet type

Fig 9A

BIT BUFFER	A8	A7	A6	A5	A4	A3	A2	A1	A0	B8	B7	B6	B5	B4	B3	B2	B1	C0	C8	C7	C6	C5	C4	C3	C2	C1	C0
BIT CONTENT	0	0	1	0	0	0	0	0	0	1	1	1	0	0	1	1	1	1	1	1	1	0	0	0	0	0	0
"10" DETECTION	/	/	/	/	/	/	/	/	/	/	/	/	/	/	/	/	/	/	/	/	/	/	/	/	/	/	/
"10" DETECTION	0	0	1	0	0	0	0	0	0	1	0	0	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0
RESULT																											
Symbol																											
STARTING POINTS																											

FIG.10

Fig 9B

910

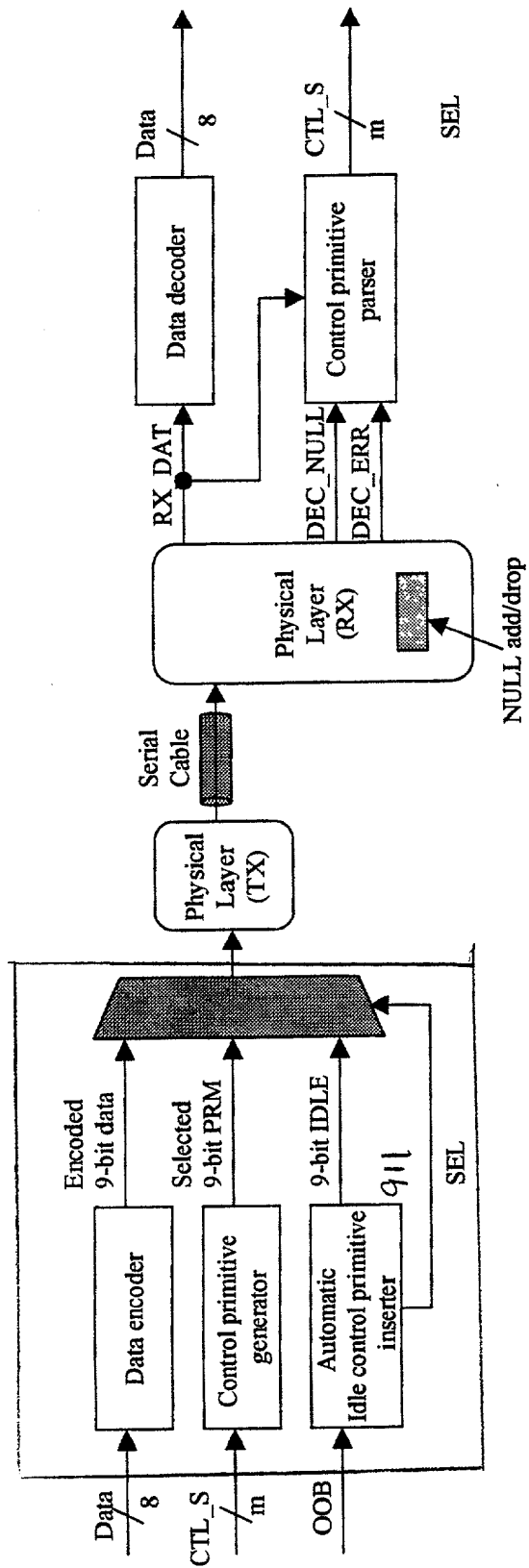


Fig. 9C

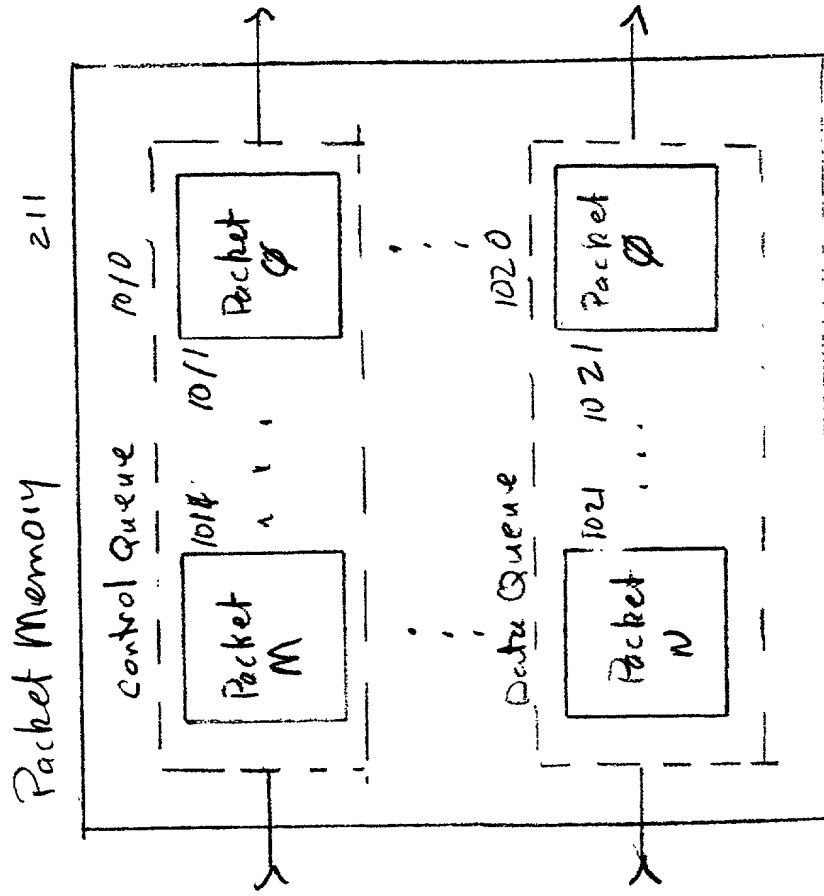


Fig 10

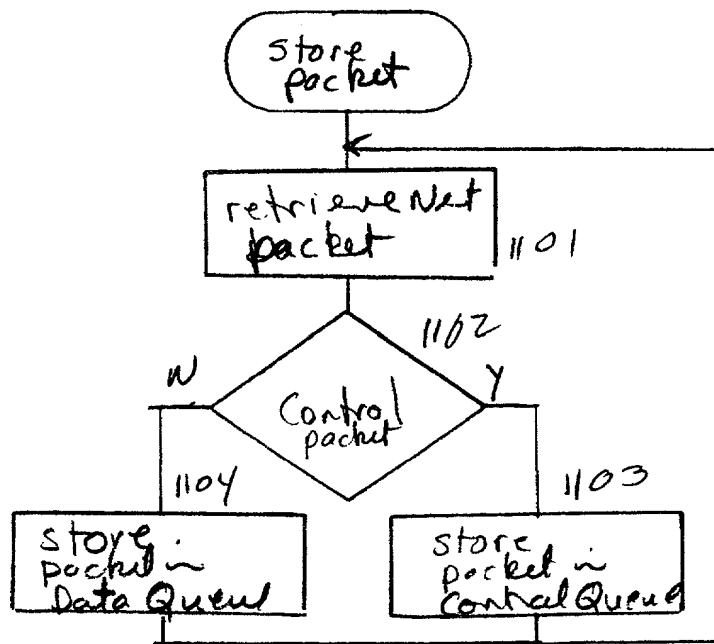


Fig 11

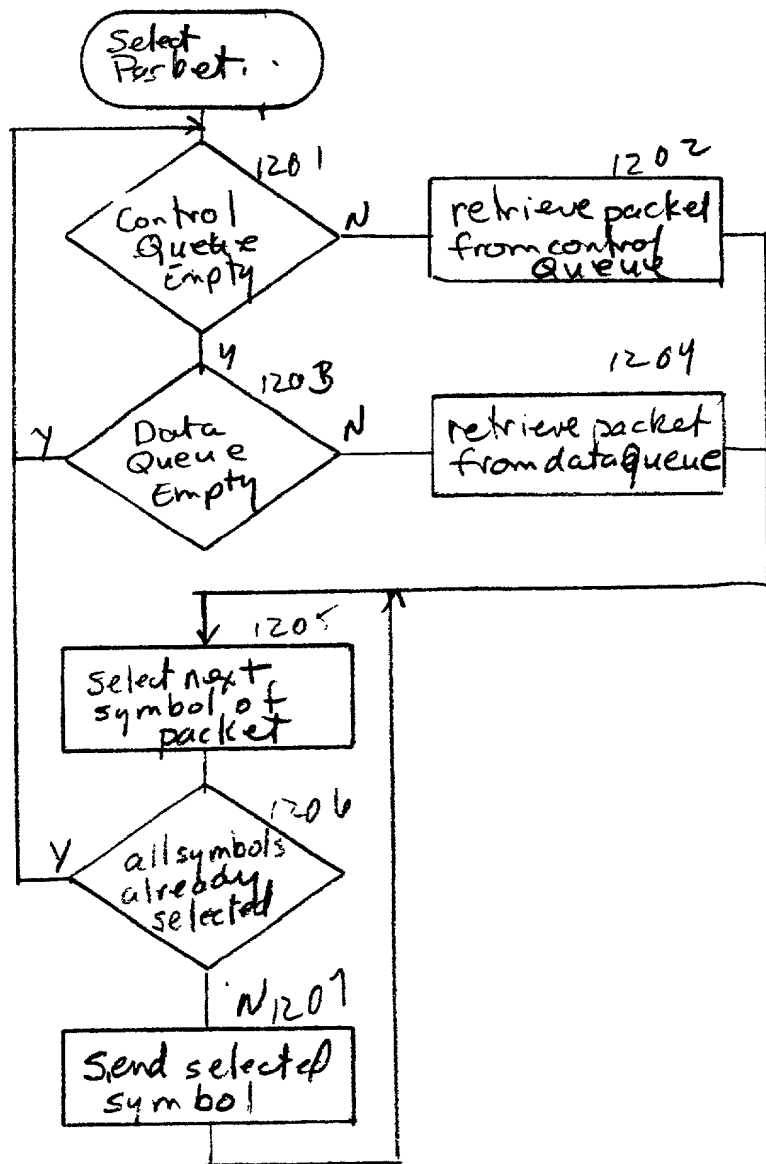


Fig 12

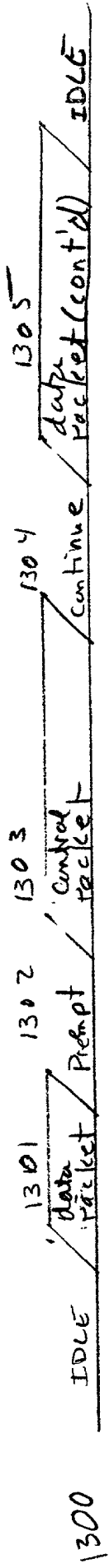


Fig 13

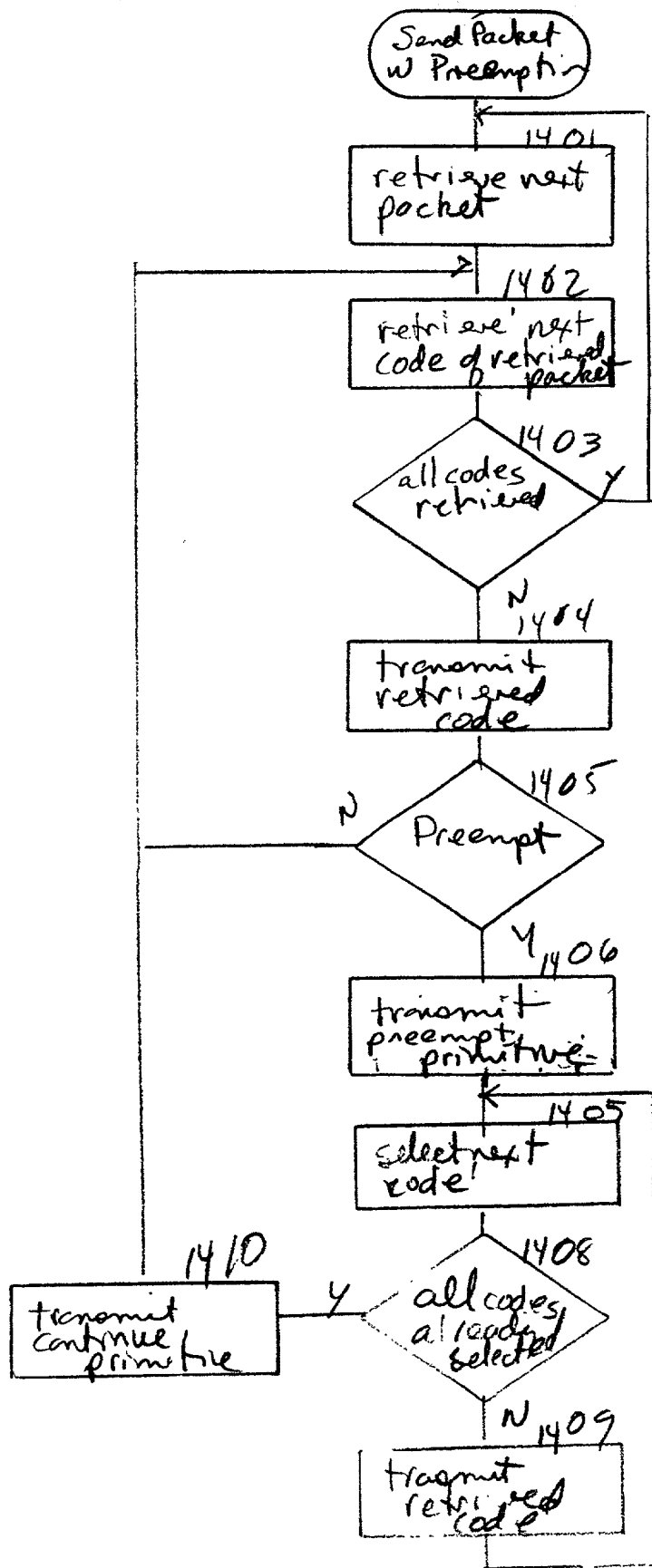


Fig 14

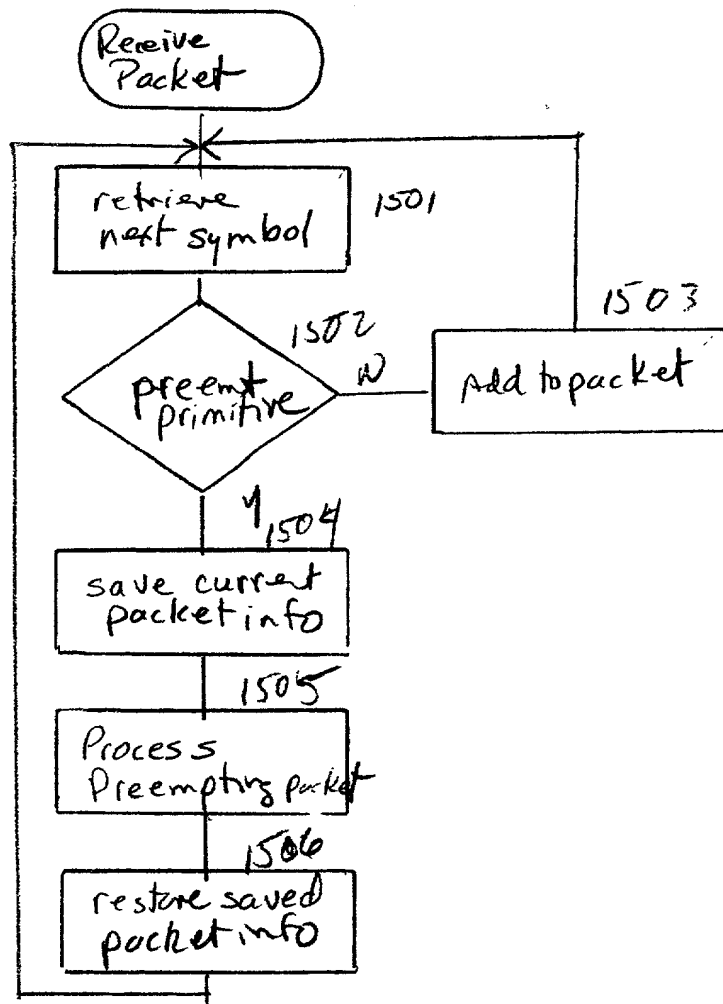


Fig 15

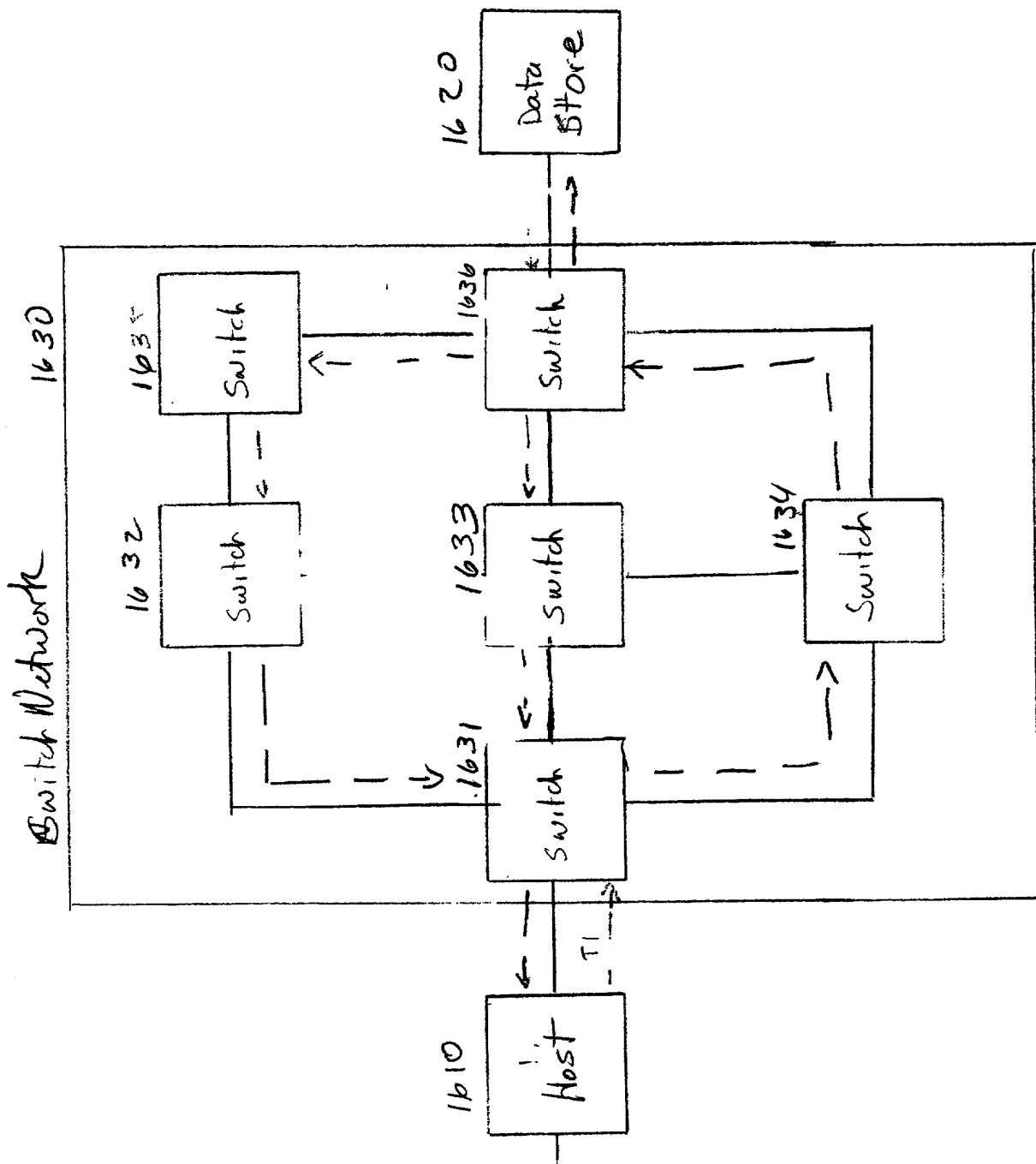
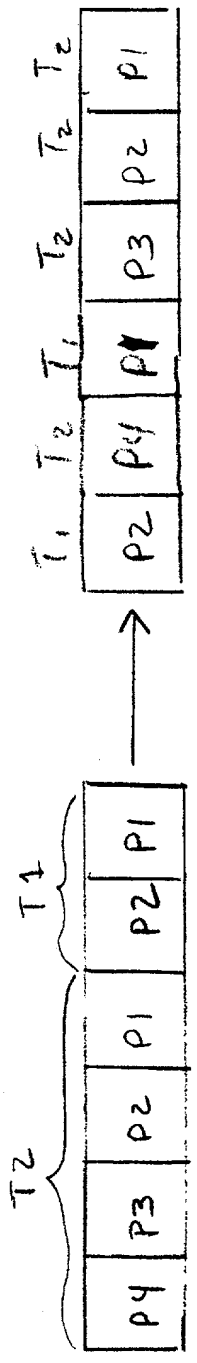


Fig 16

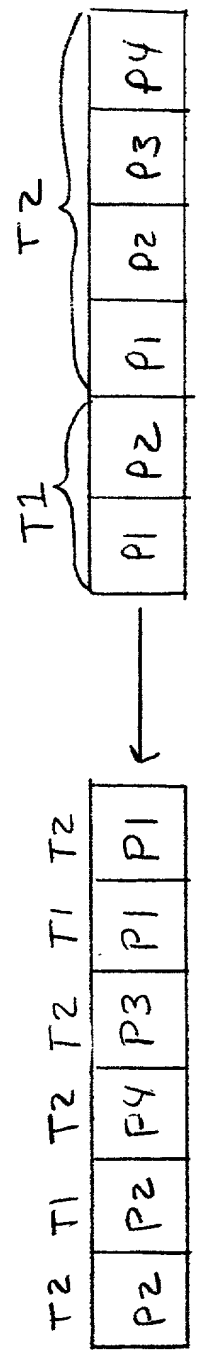
TOGETHER Data Store

Host



1701

Preserving Packet Order w/ Transaction



1702

No Packet or Transaction Ordering

Fig 17

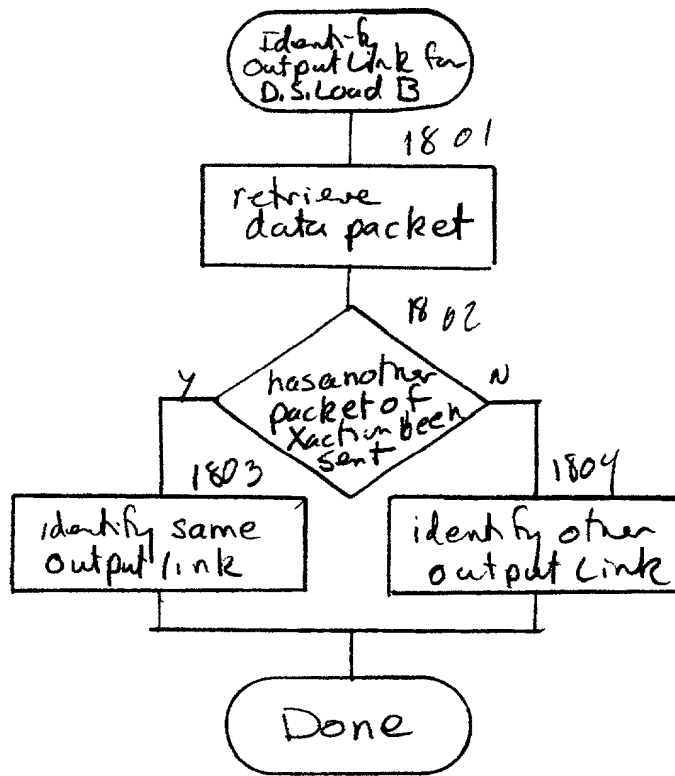


Fig 18

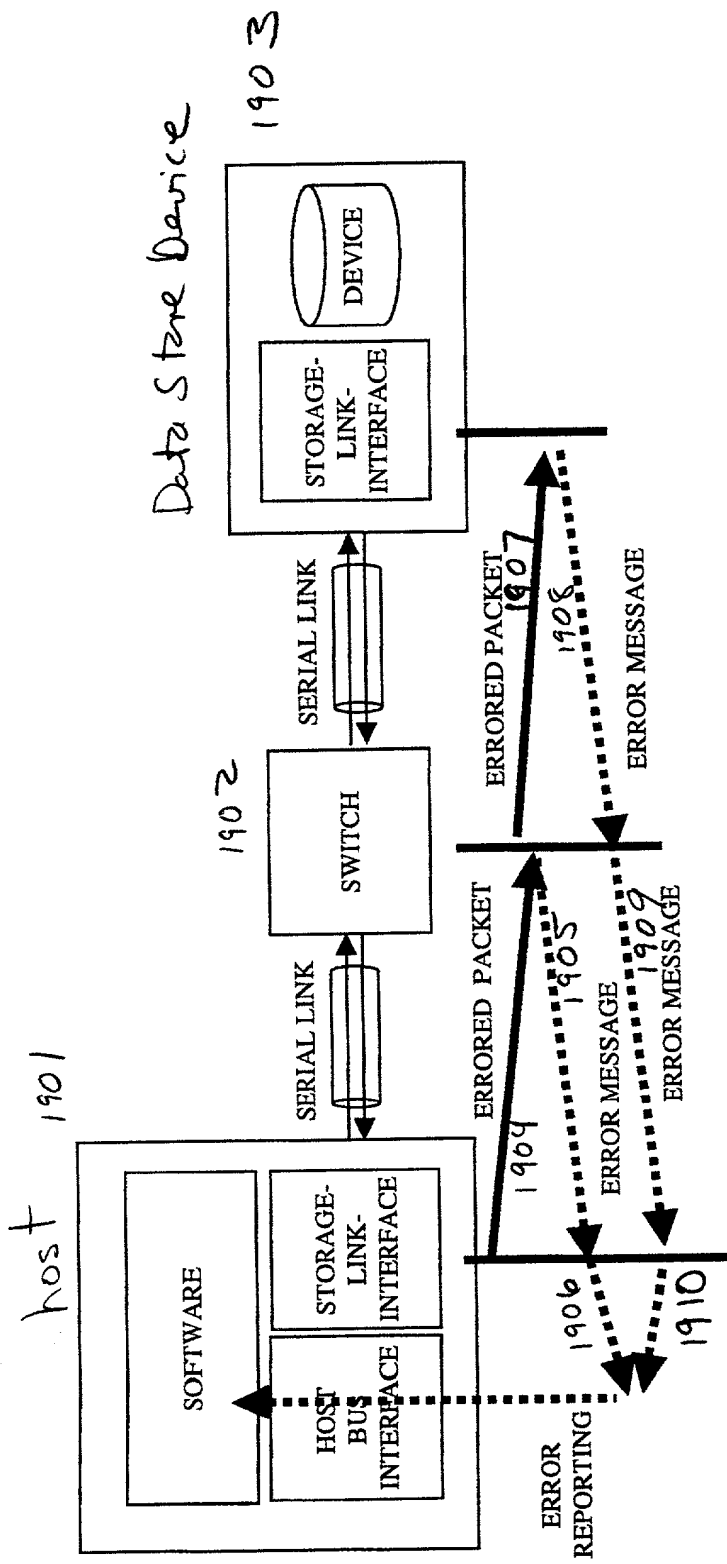


Fig 19A

~~TOP SECRET~~

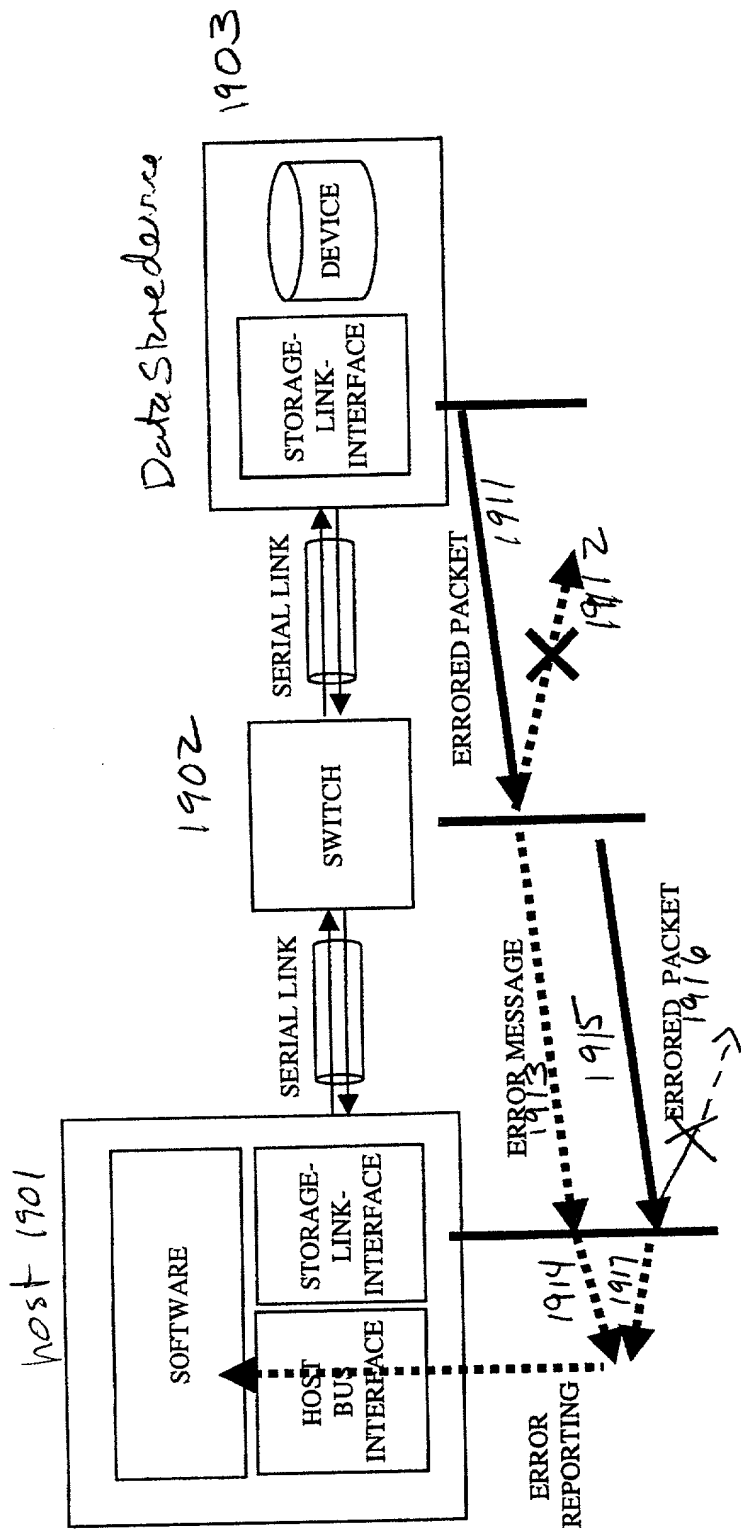
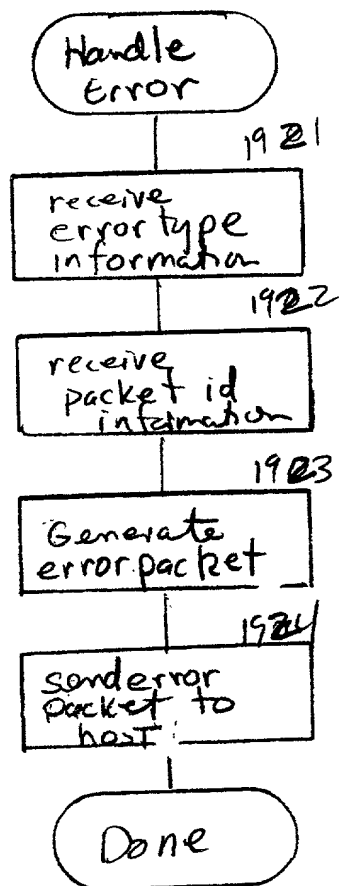


Fig 19B



19C

Block
Disparity
+ 4

Symbol
I

101010101

Alternate
Bit
Inversion

00000000

Symbol
2

001110110

Symbol
3

10101010111

Bit
Inversion

11000100101010000010101

Symbol
4

110101010

Fig 21A

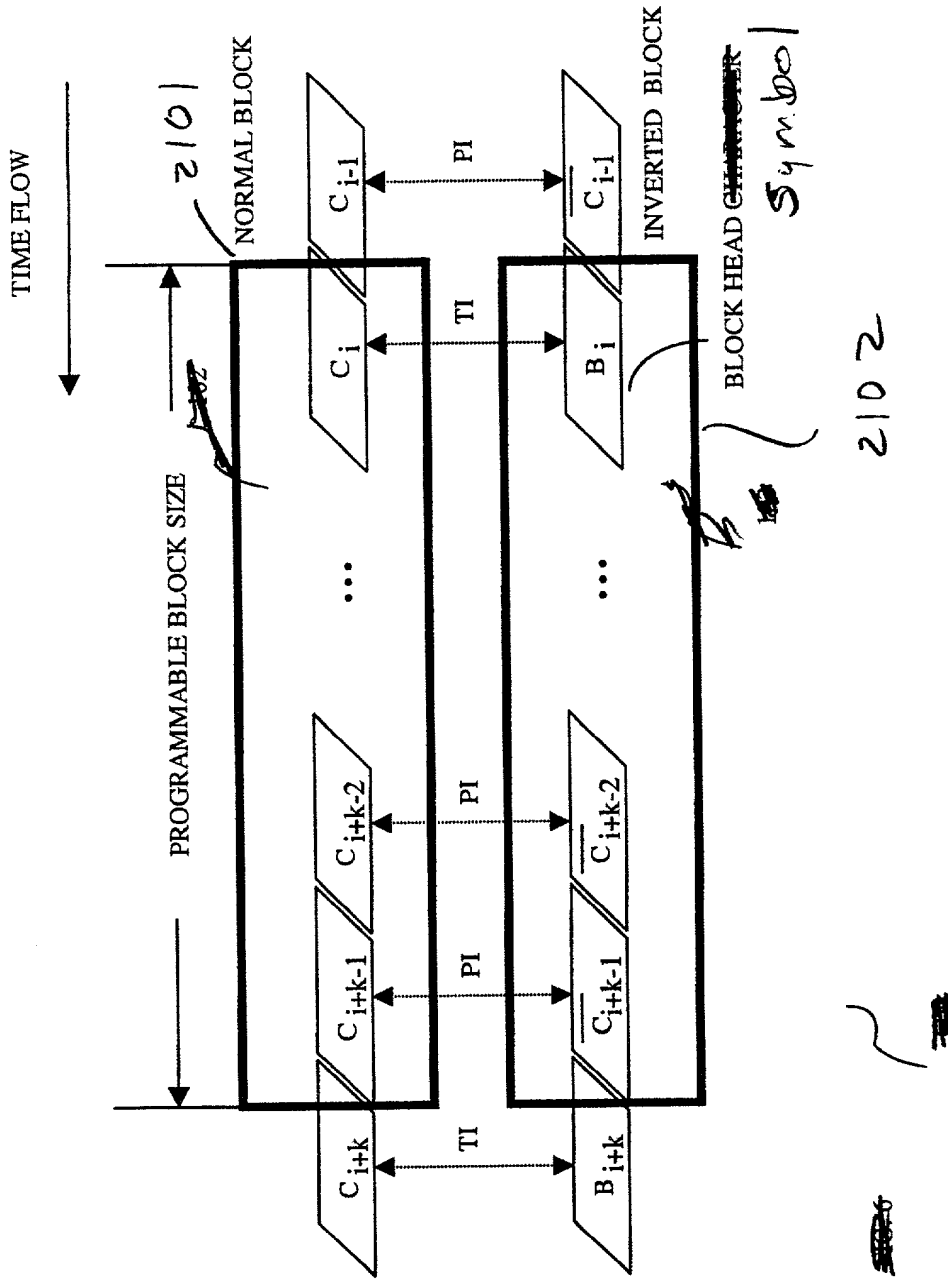


Fig 21B

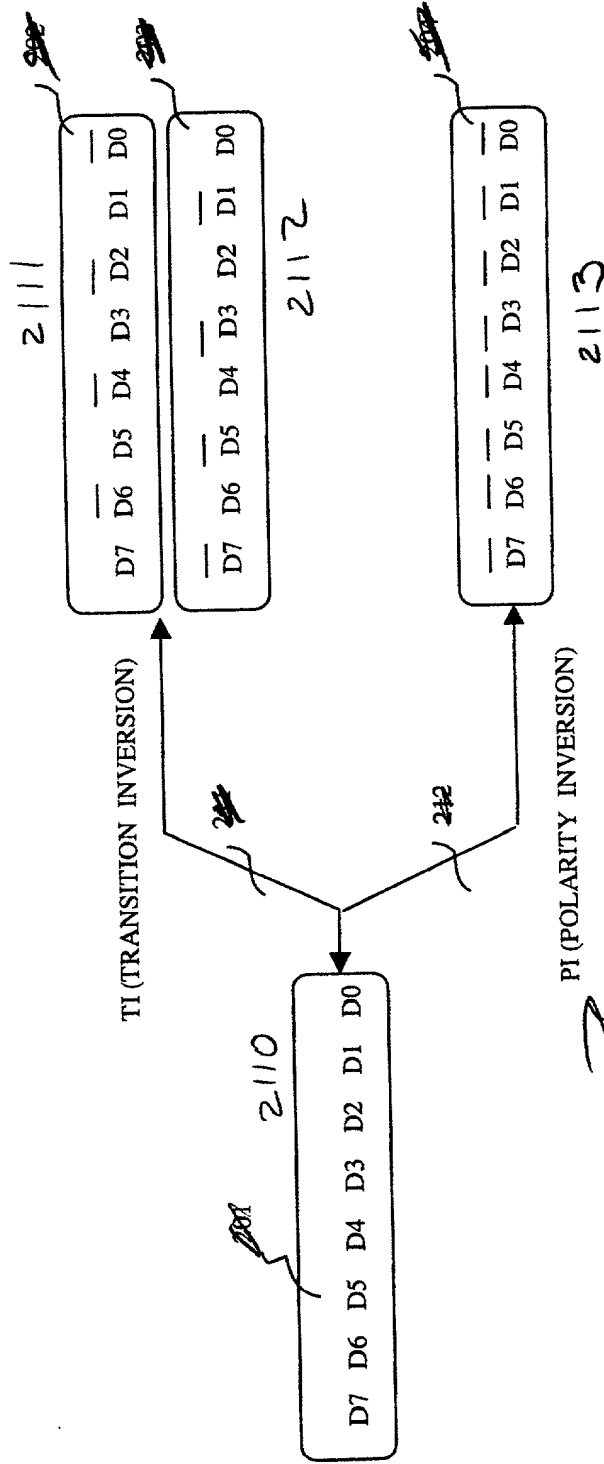


Fig 21C

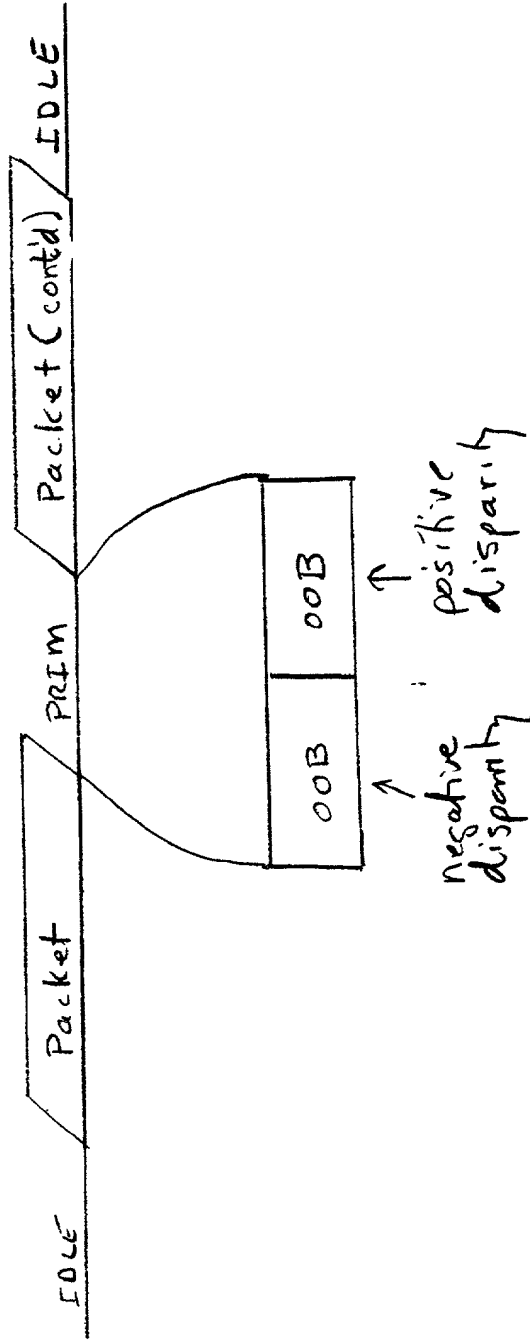


Fig 22

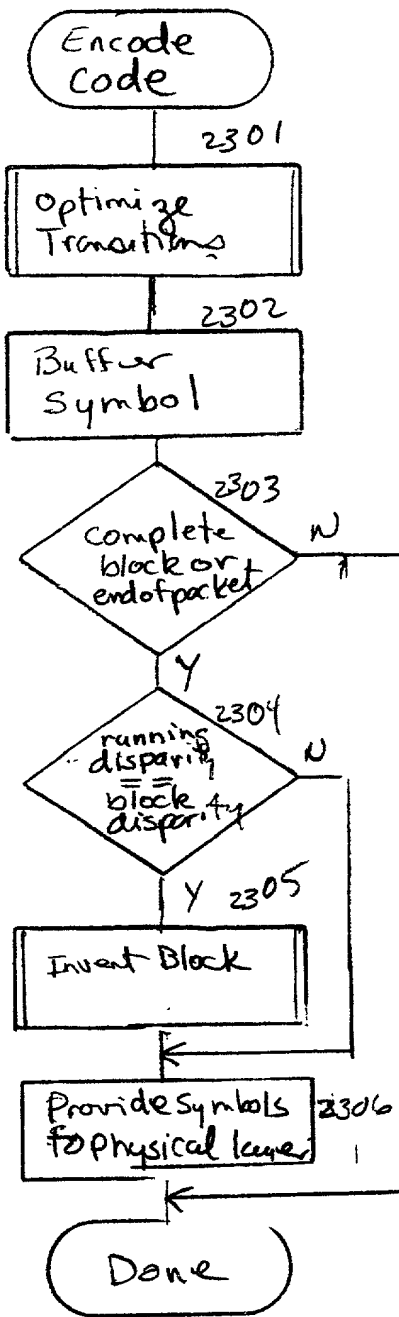


Fig 23

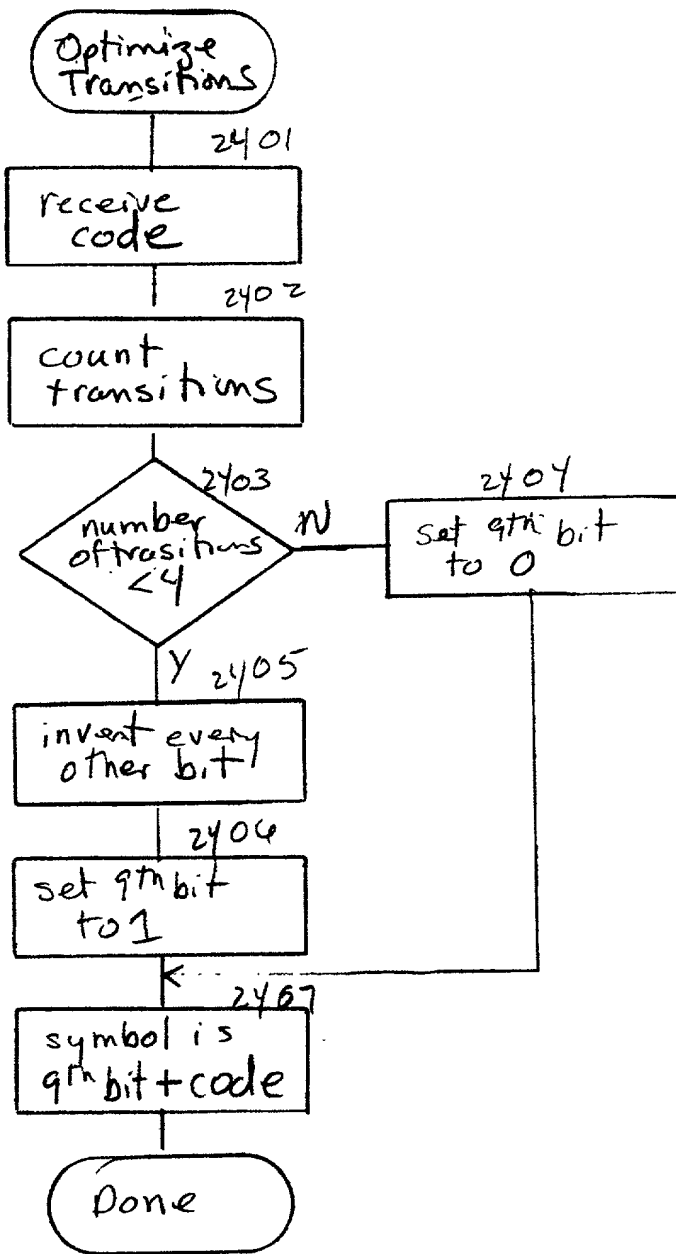


Fig 24

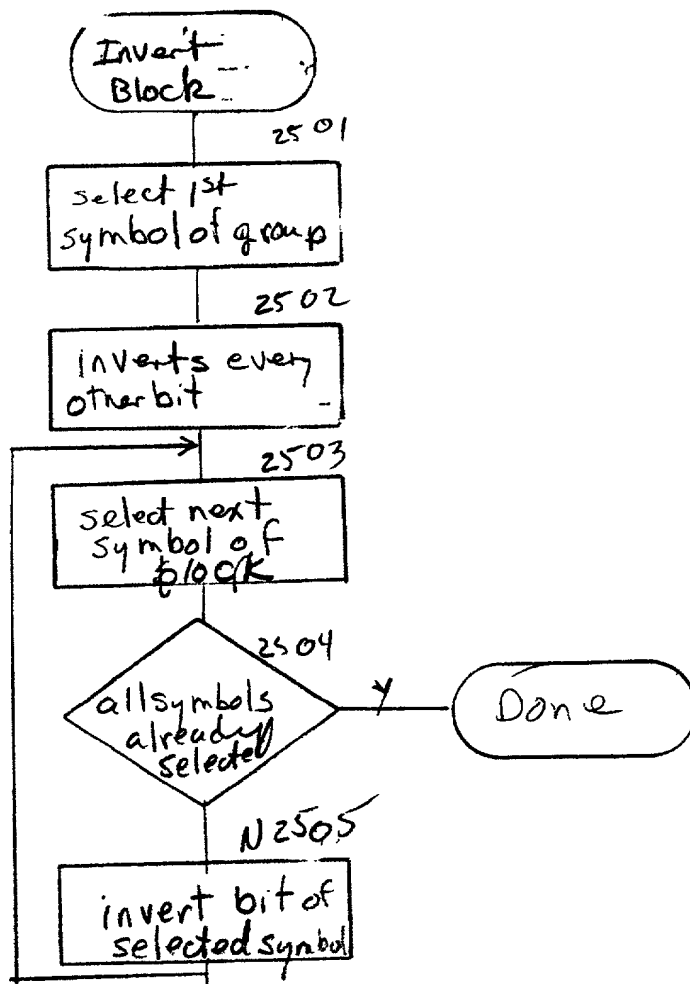


Fig 25

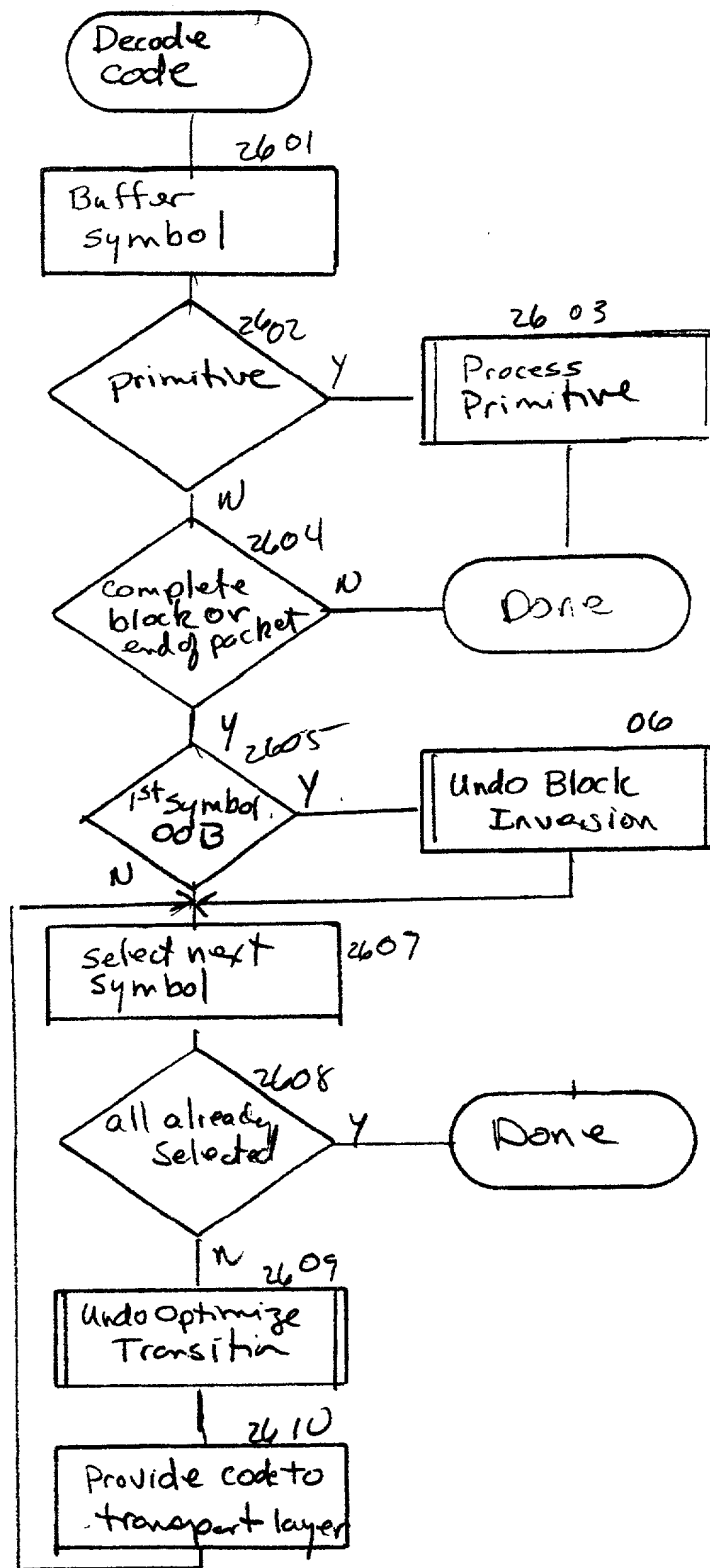


Fig 26

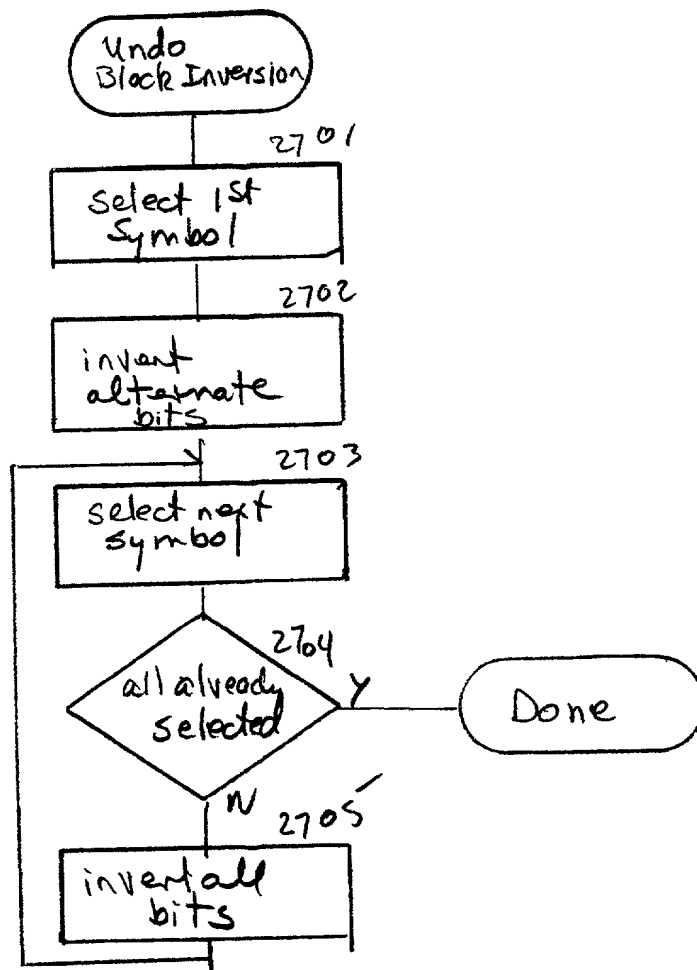


Fig 27

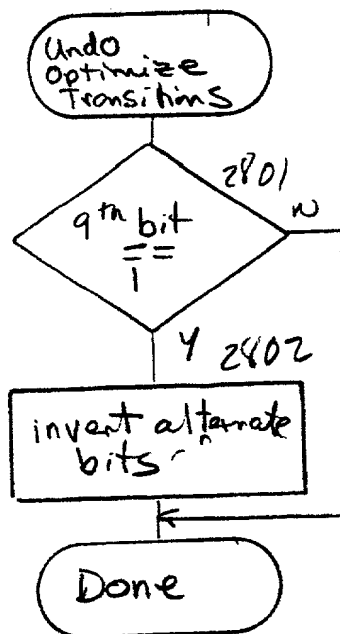


Fig 28

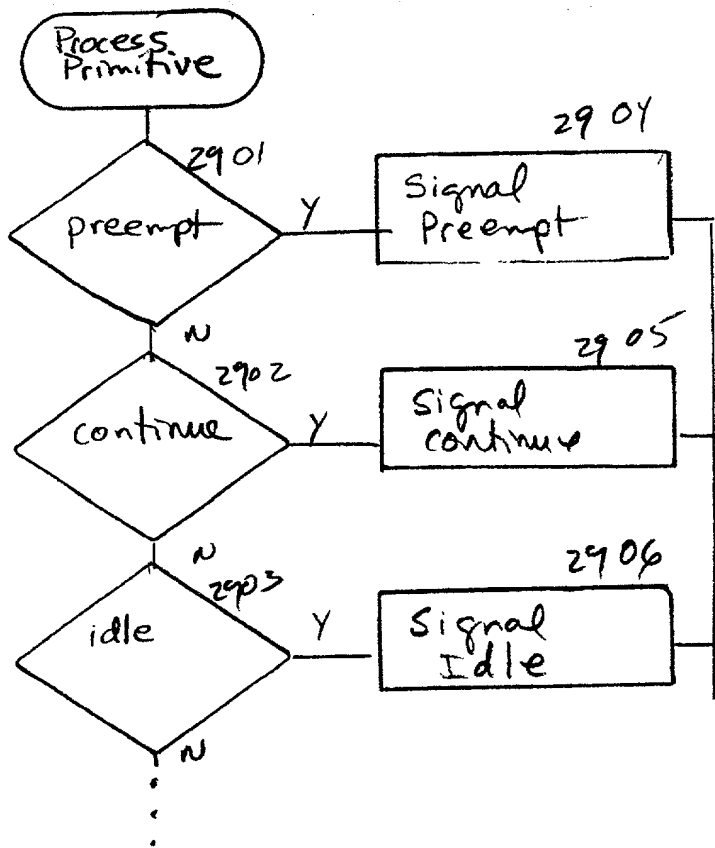


Fig 29

Multipoint Memory Device 3000

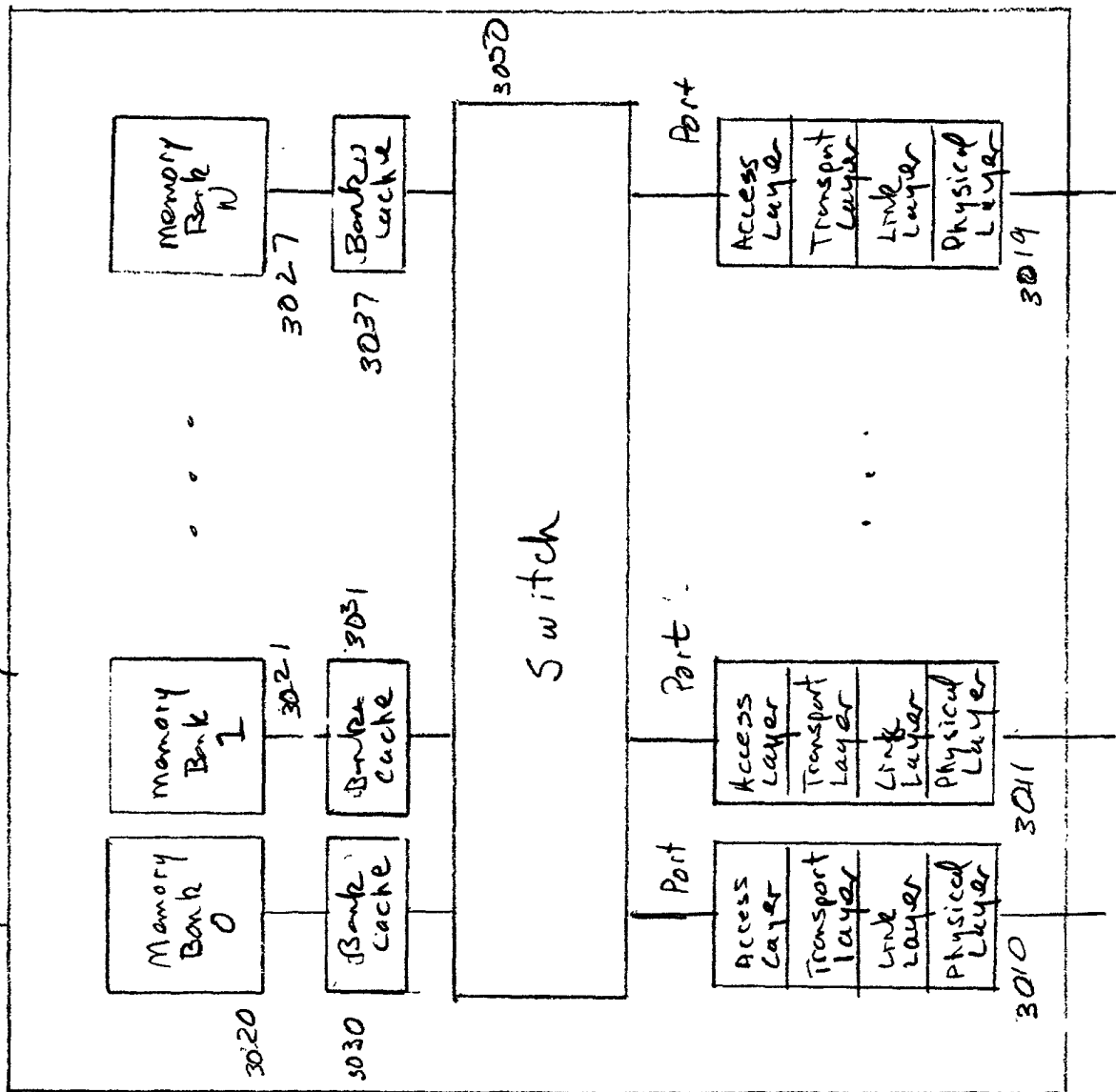


Fig 30

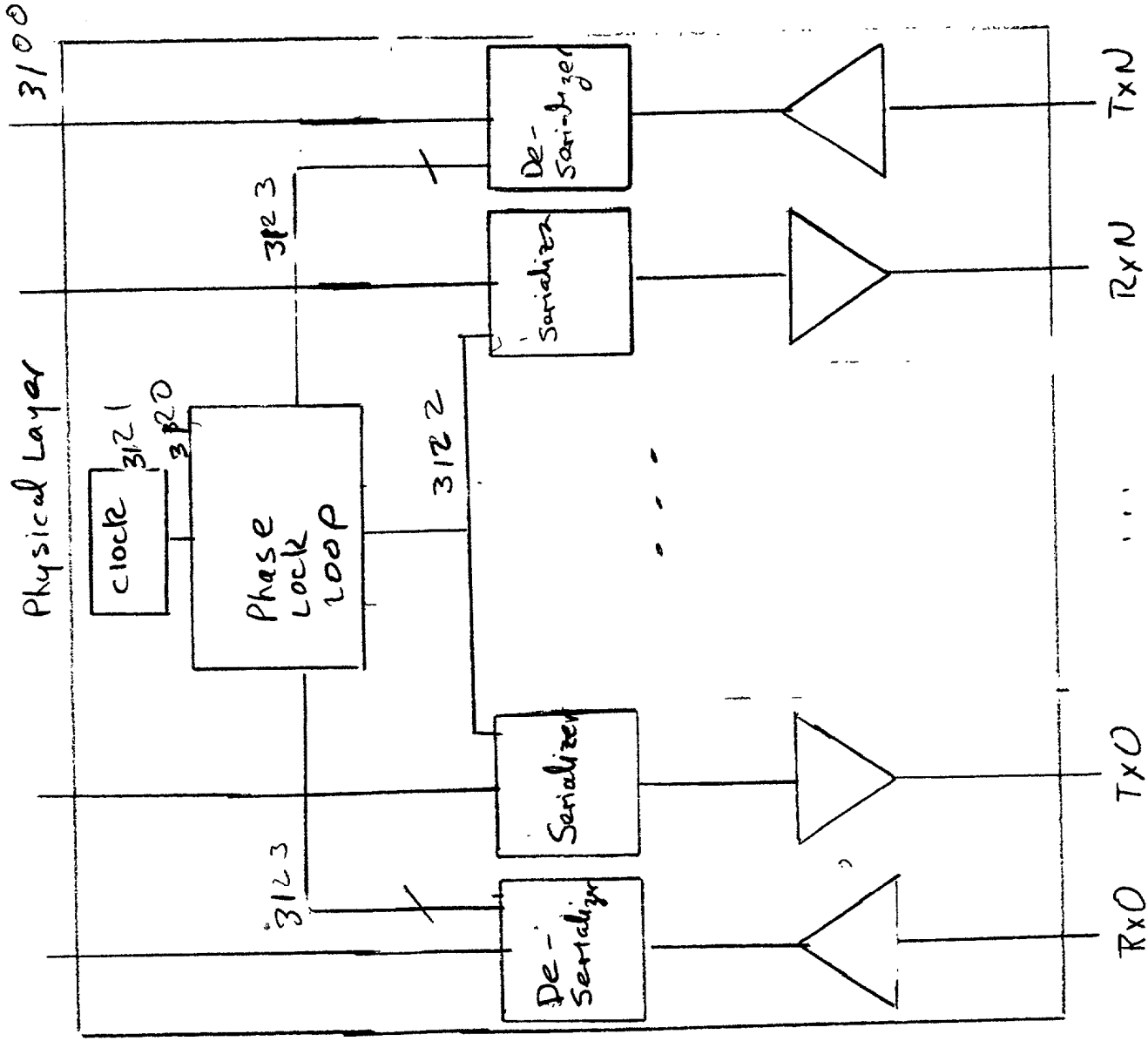


FIG. 31

Input Queue 3201				Output Queue 3202			
Port	R/W	Address	Data	Valid	Port	Data	
3	R	1000		1	3	11...0	
4	W	4000	10...1	0			
3	W	1000	111...0	0			
3	R	2000		1	3	101...1	
					⋮		

Fig 32

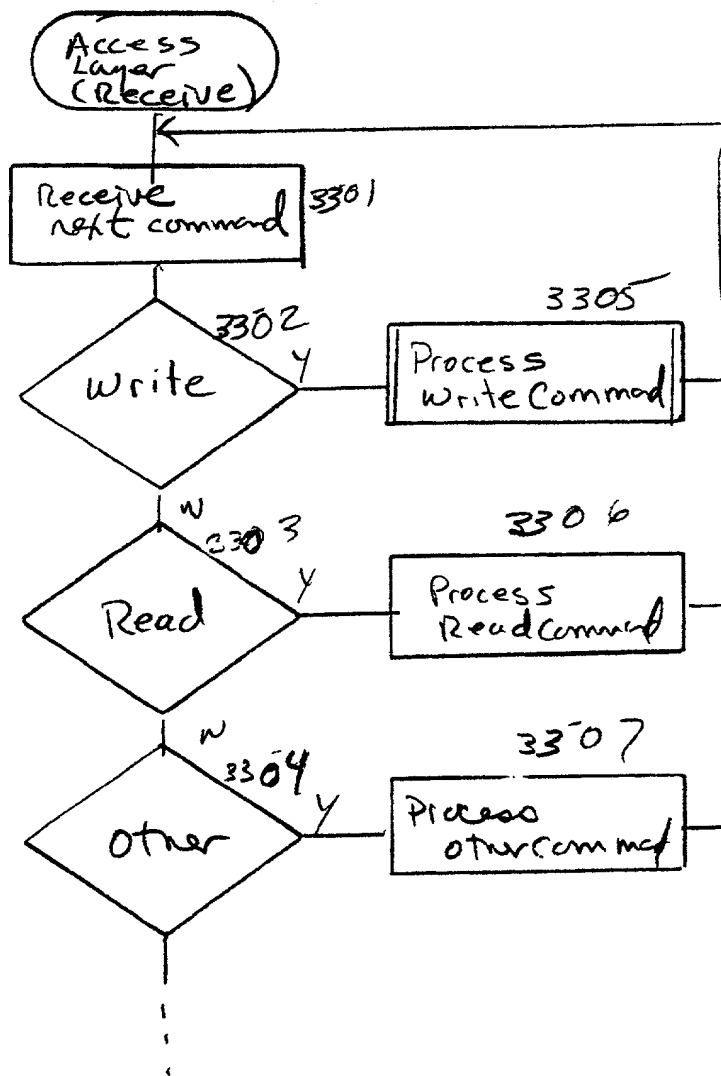


Fig 33

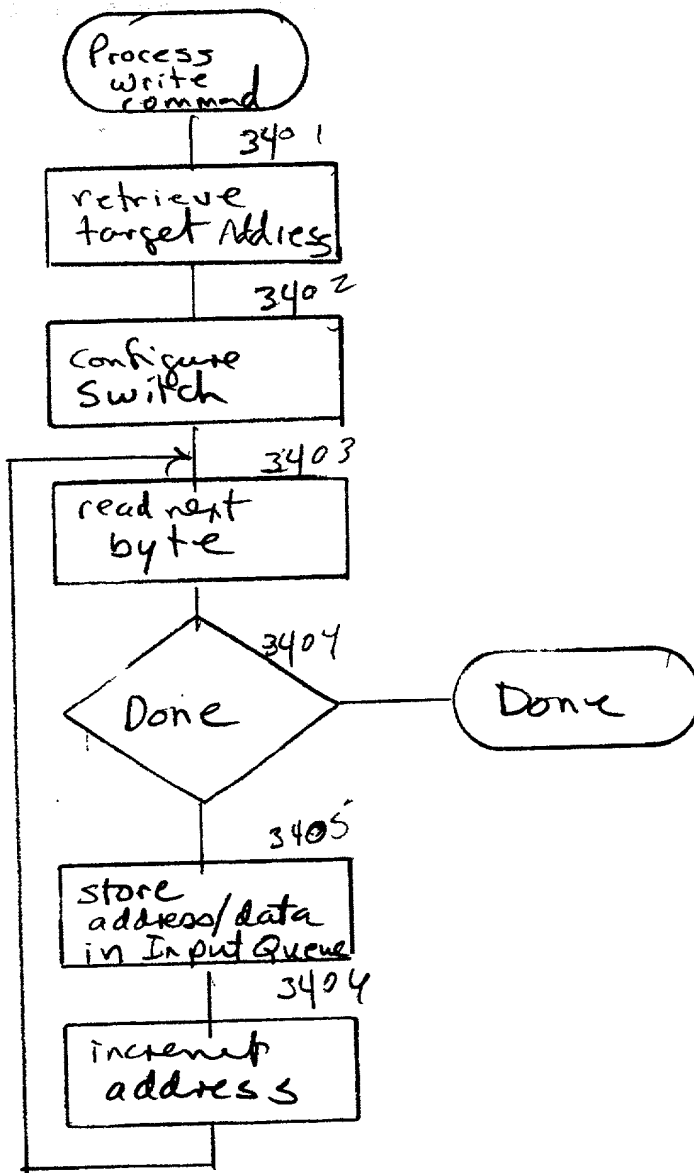


Fig 34

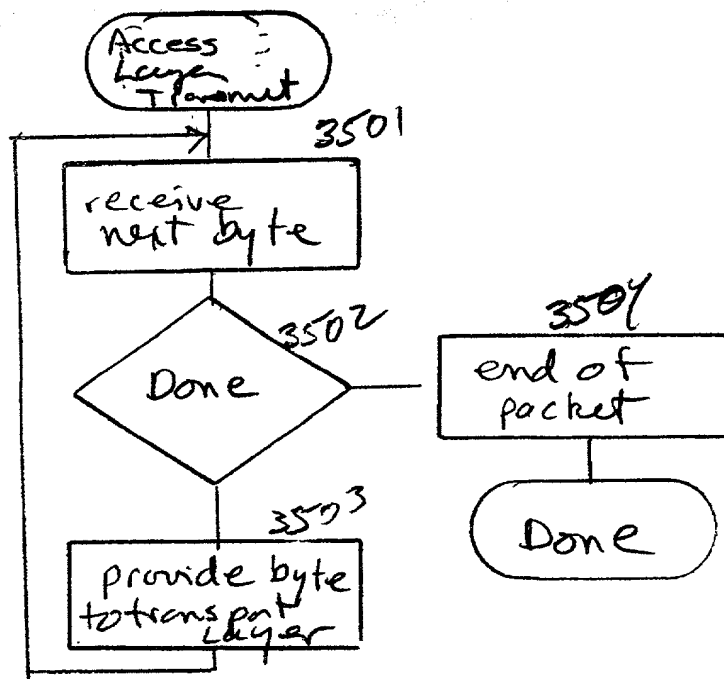


Fig 35

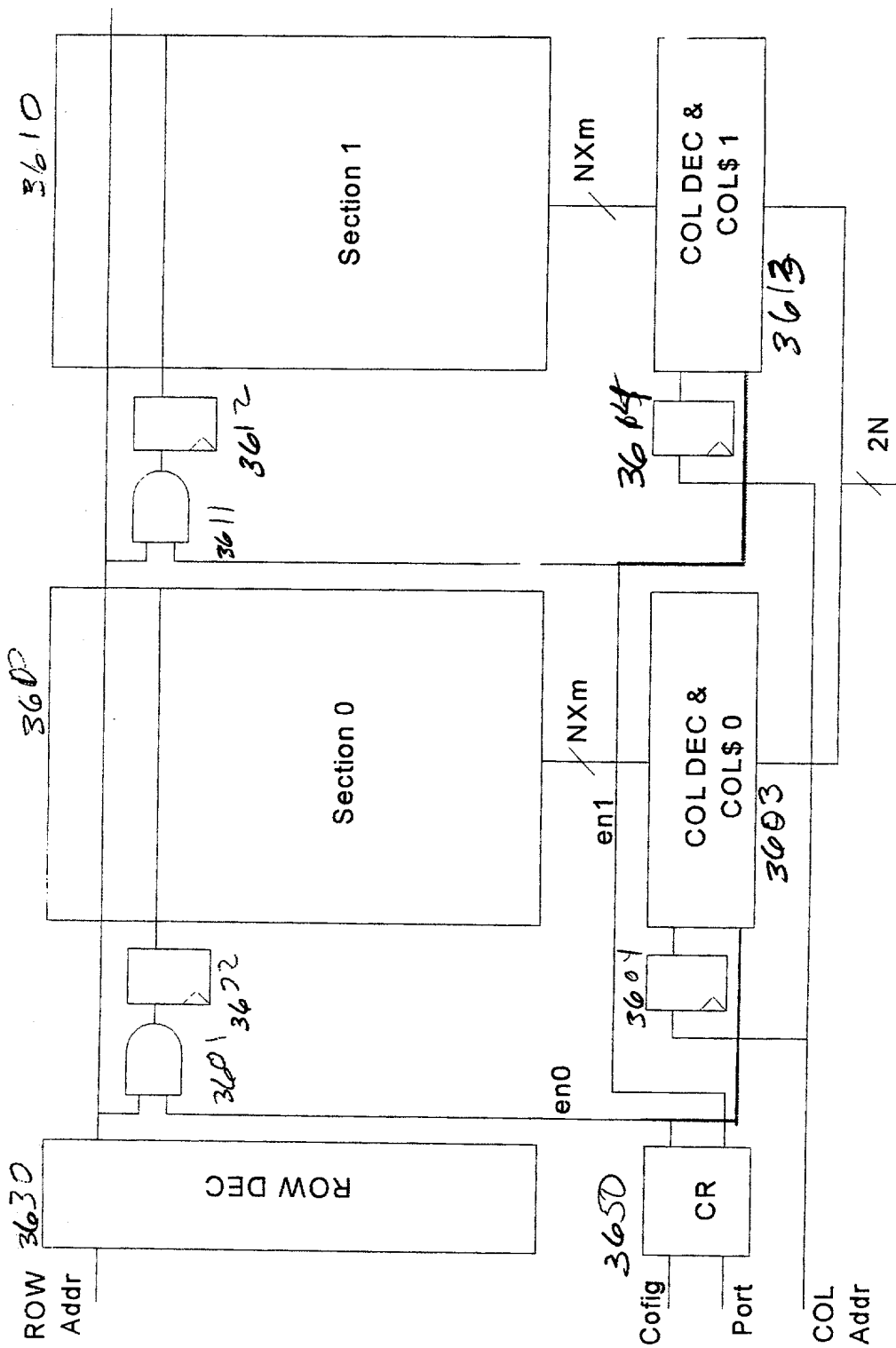
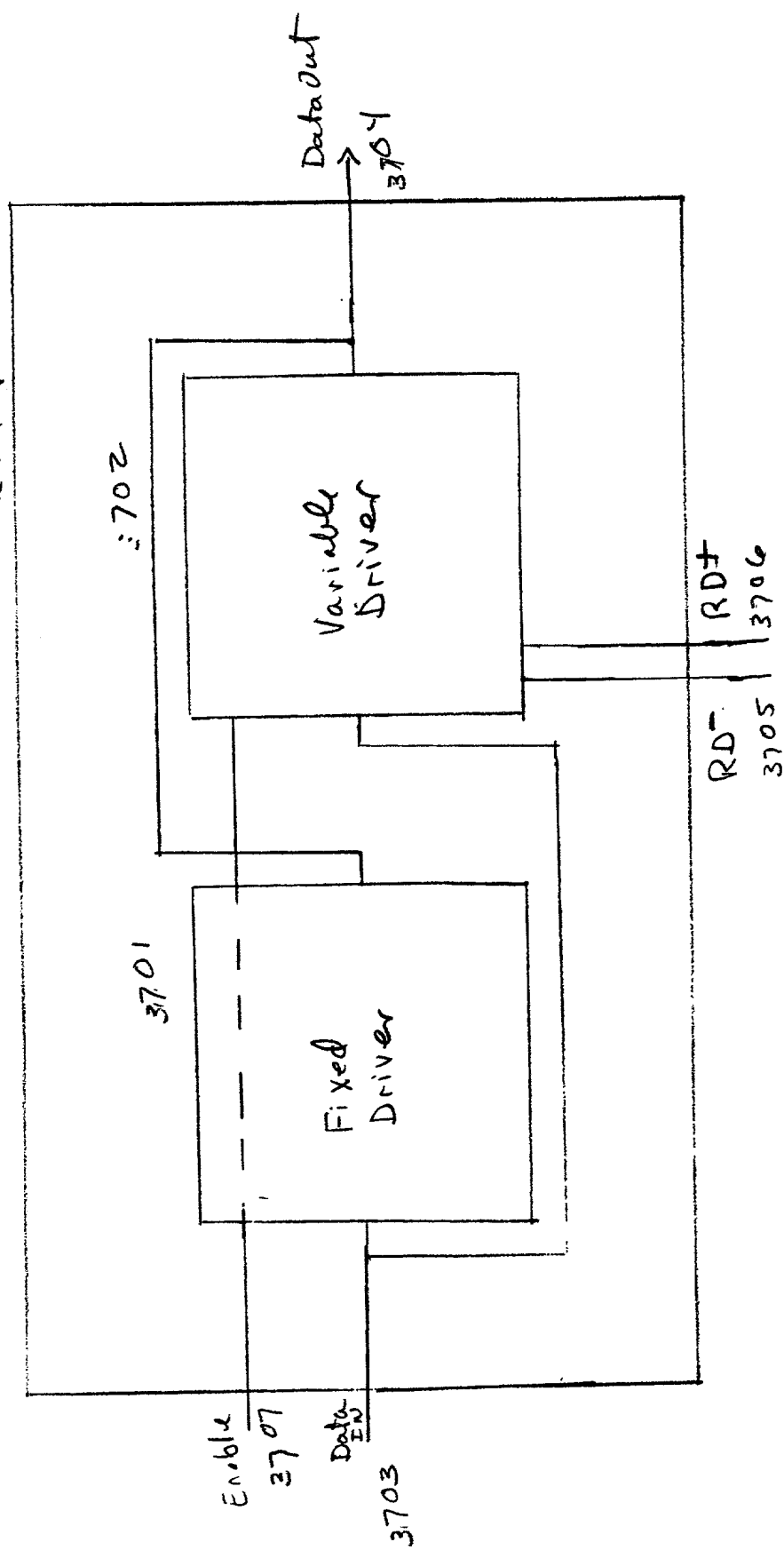


Fig 36

Line Driver 3700



Variable Driver

$\begin{cases} RD^+ \wedge \overline{DataIn} = \text{pull down} \\ RD^- \wedge DataIn = \text{pull up} \end{cases}$

Fig 37A

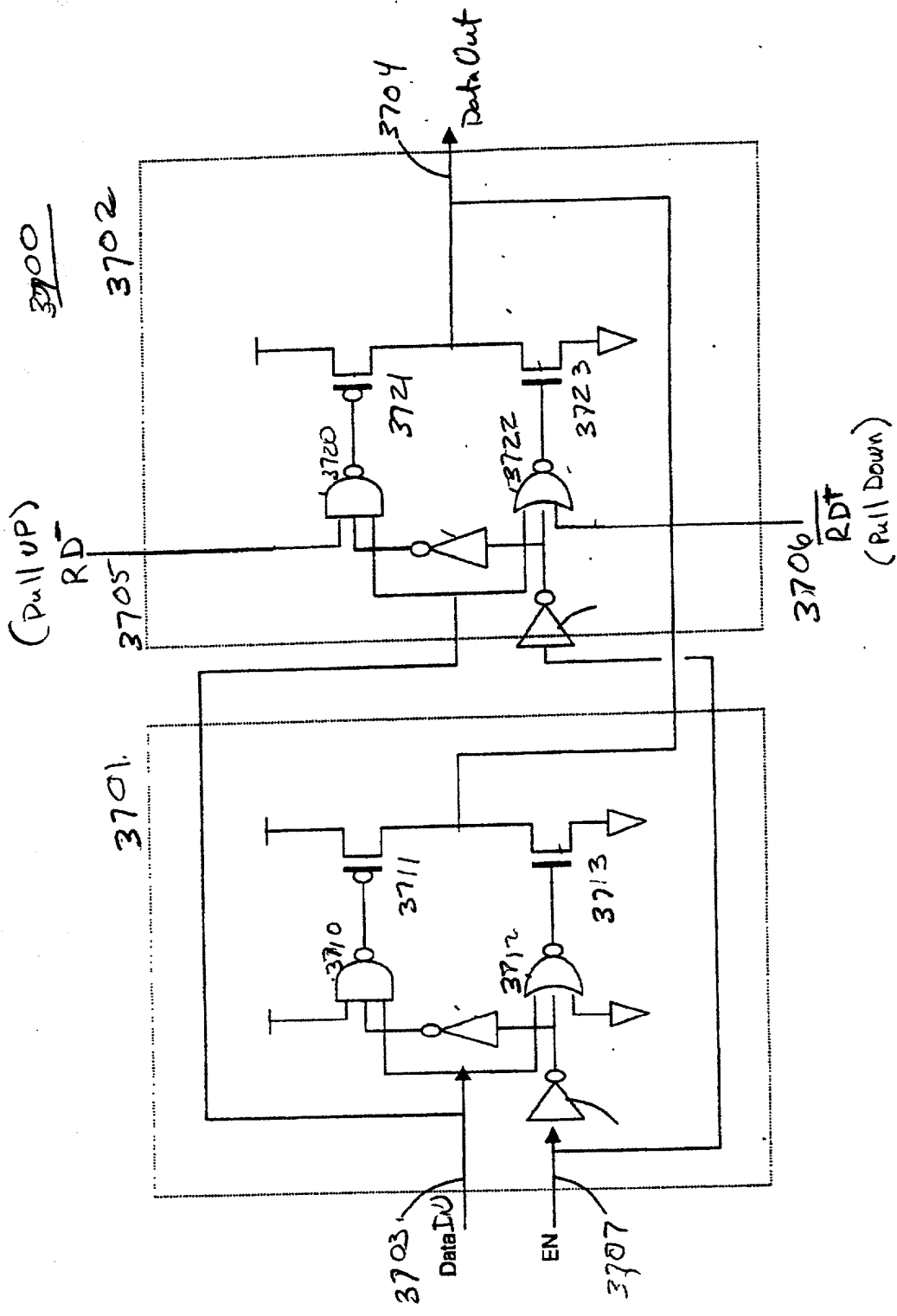


Fig 37B

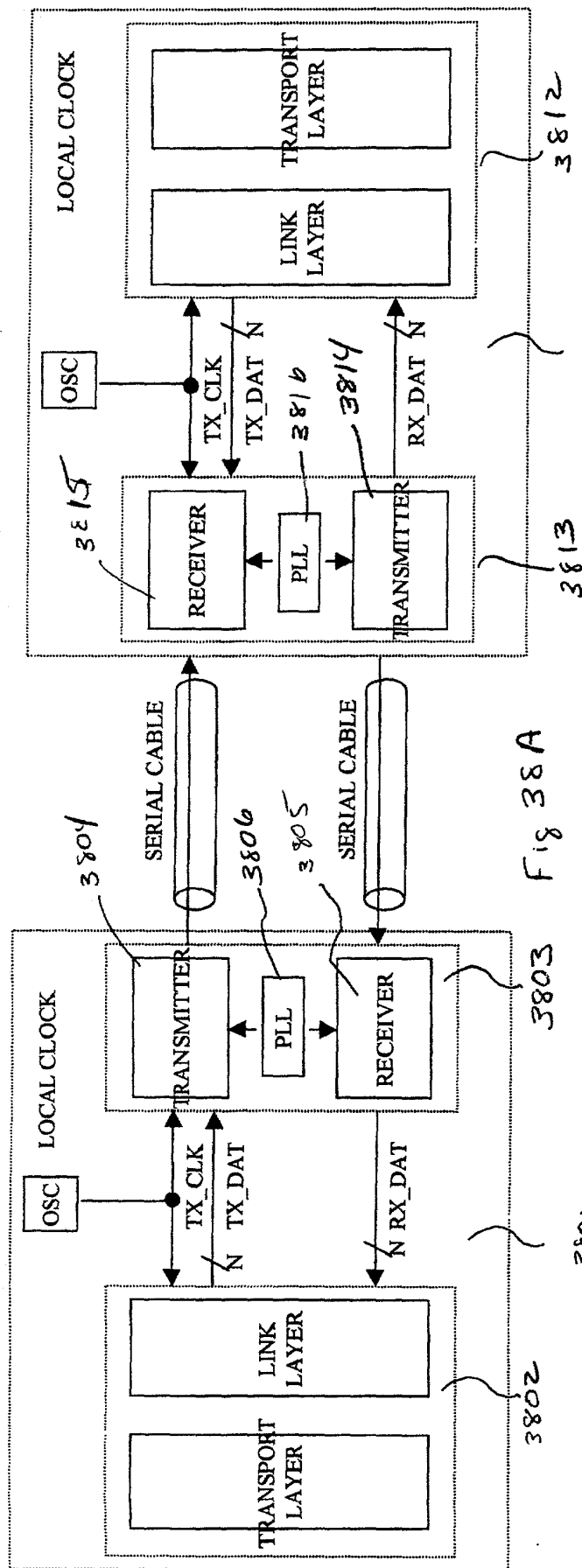


Fig 38A

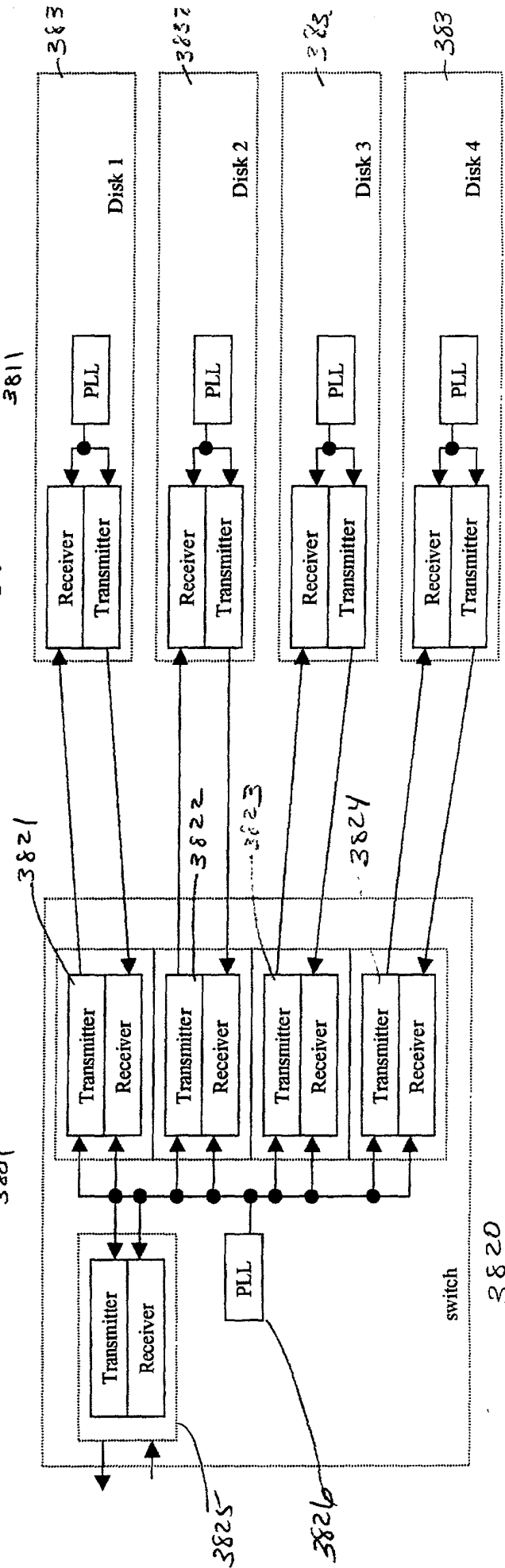
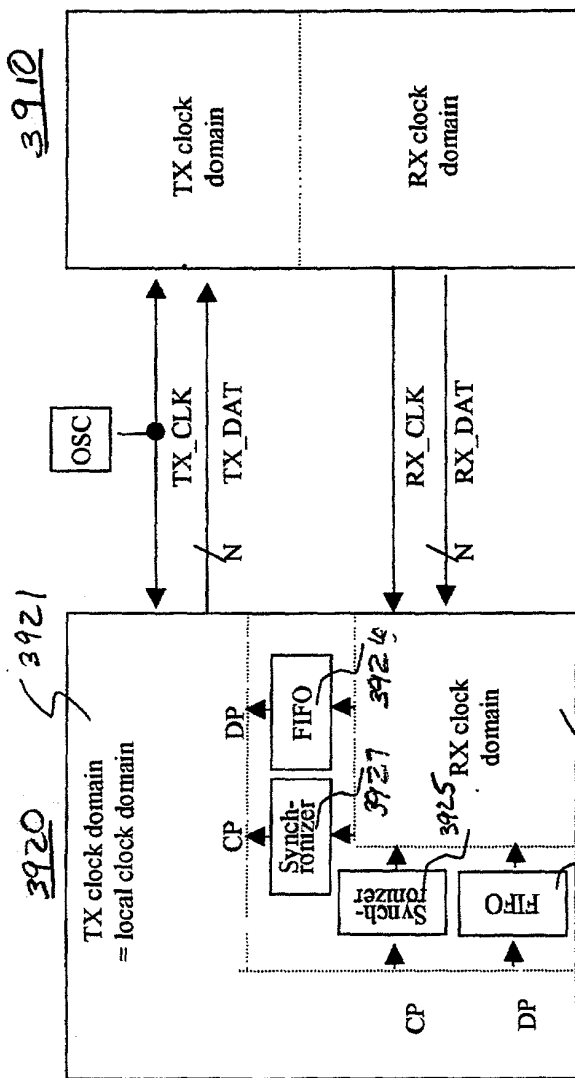


Fig 38B



Serial storage channel

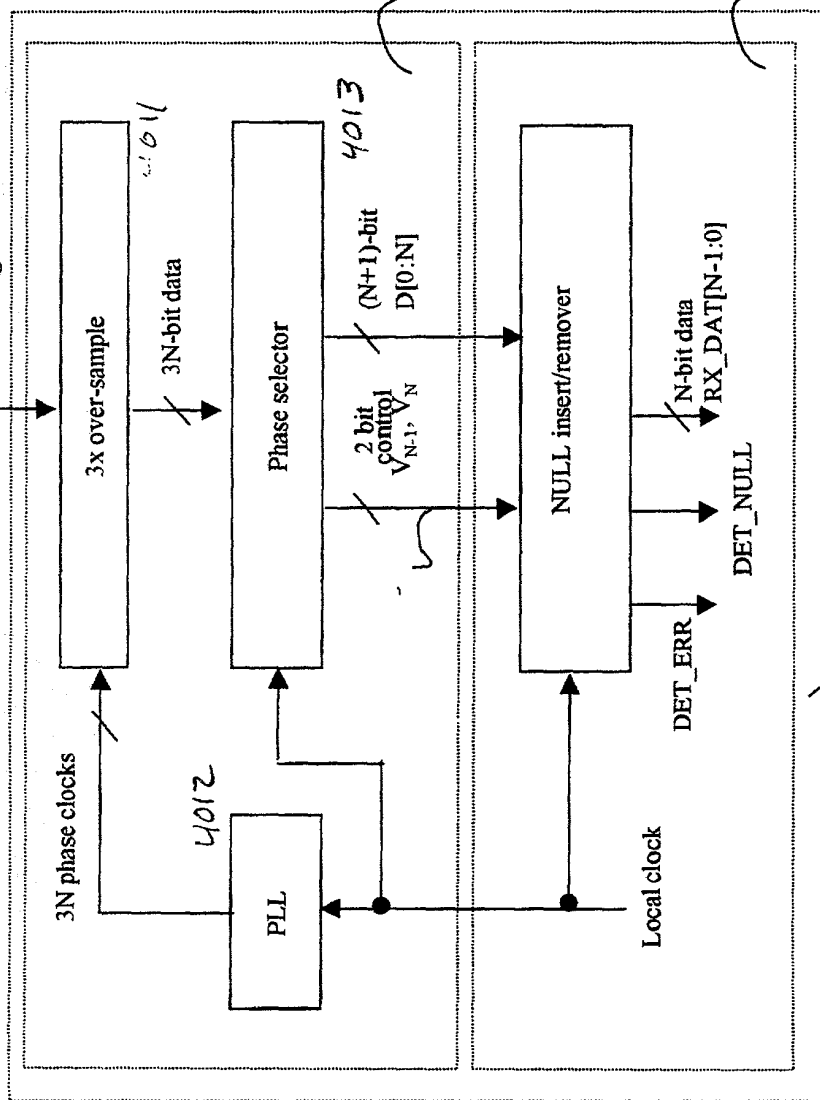


Fig 40

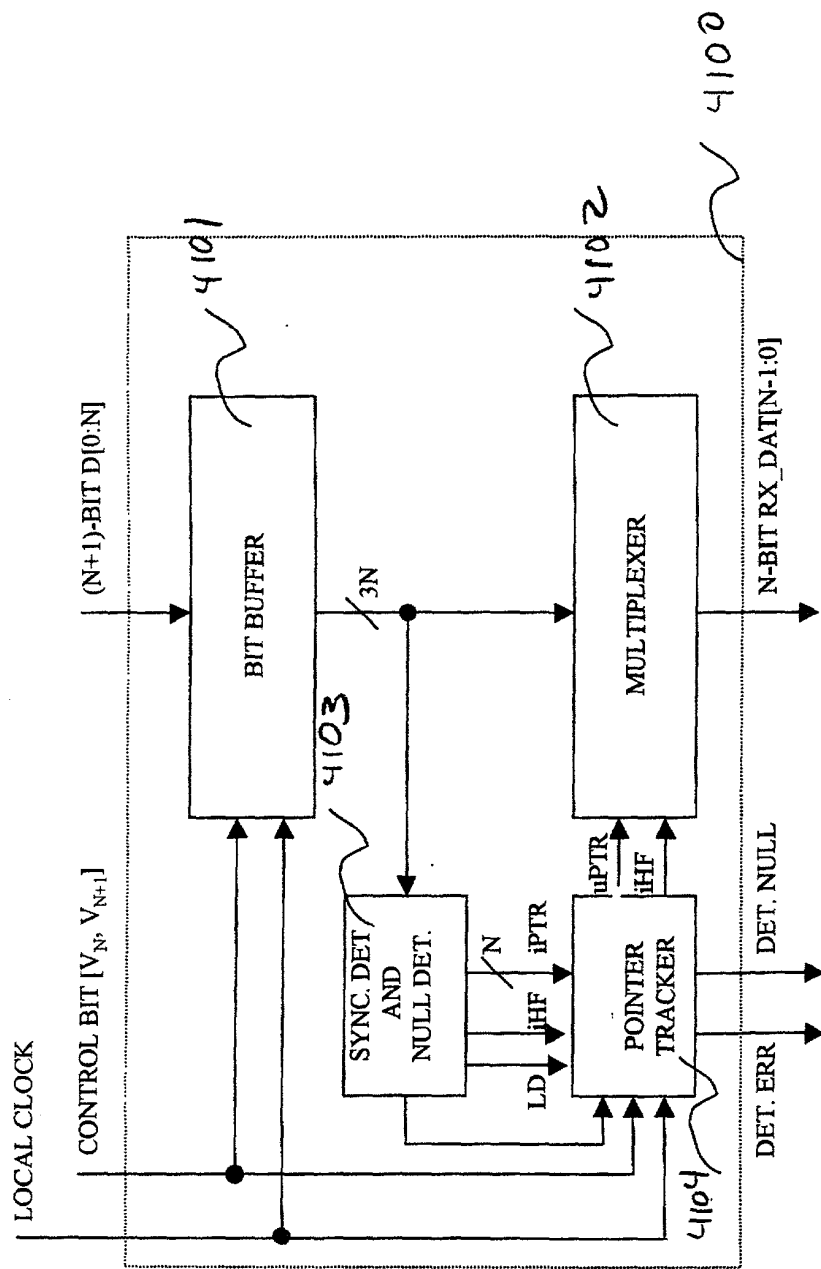


Fig 41

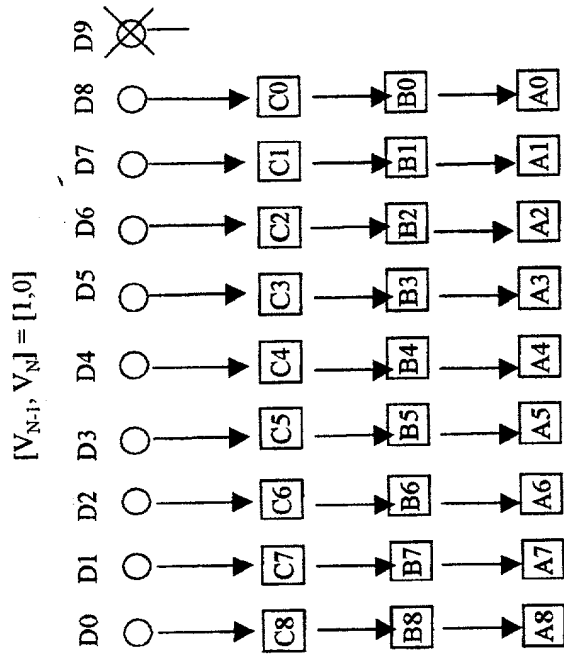


Fig 42A

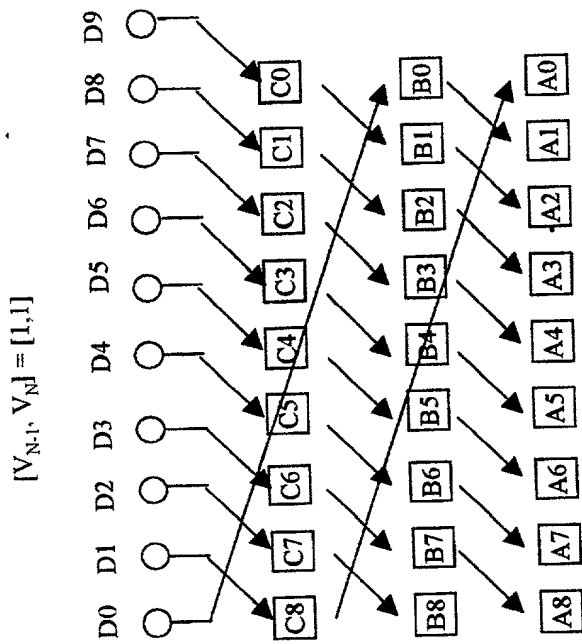


Fig 42c

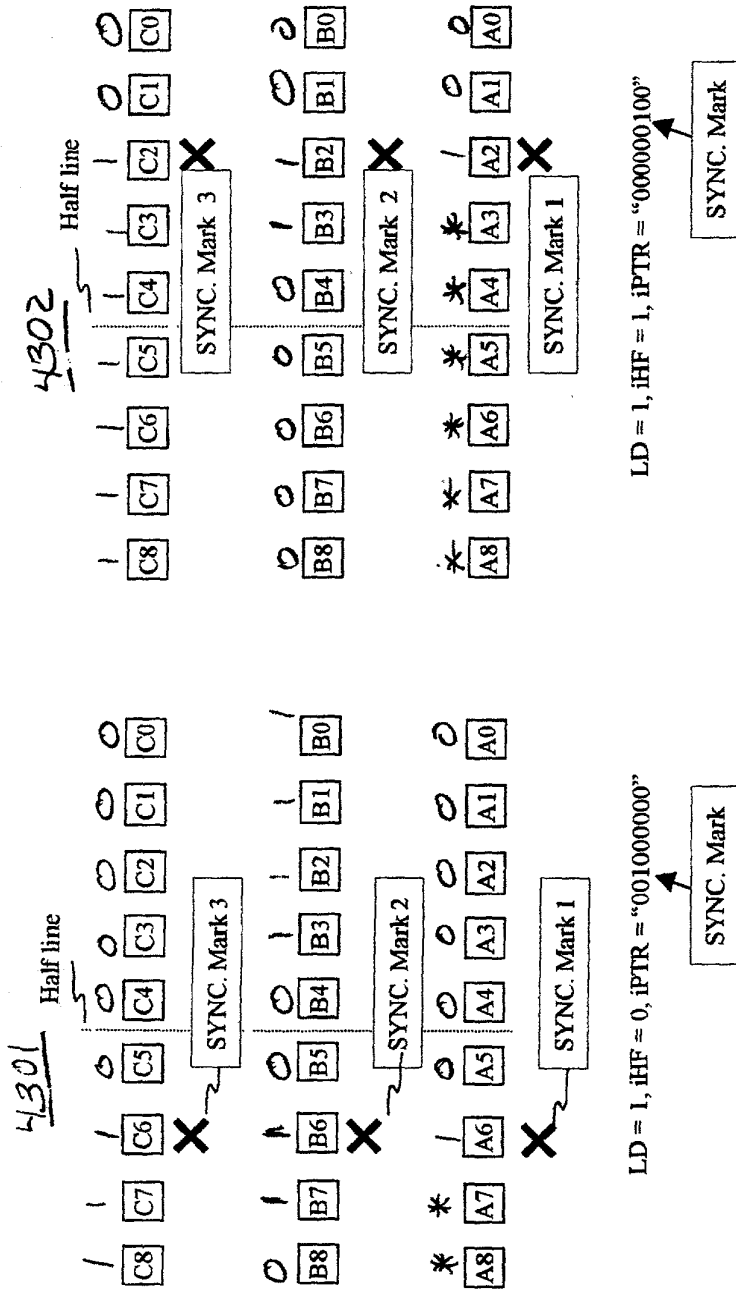
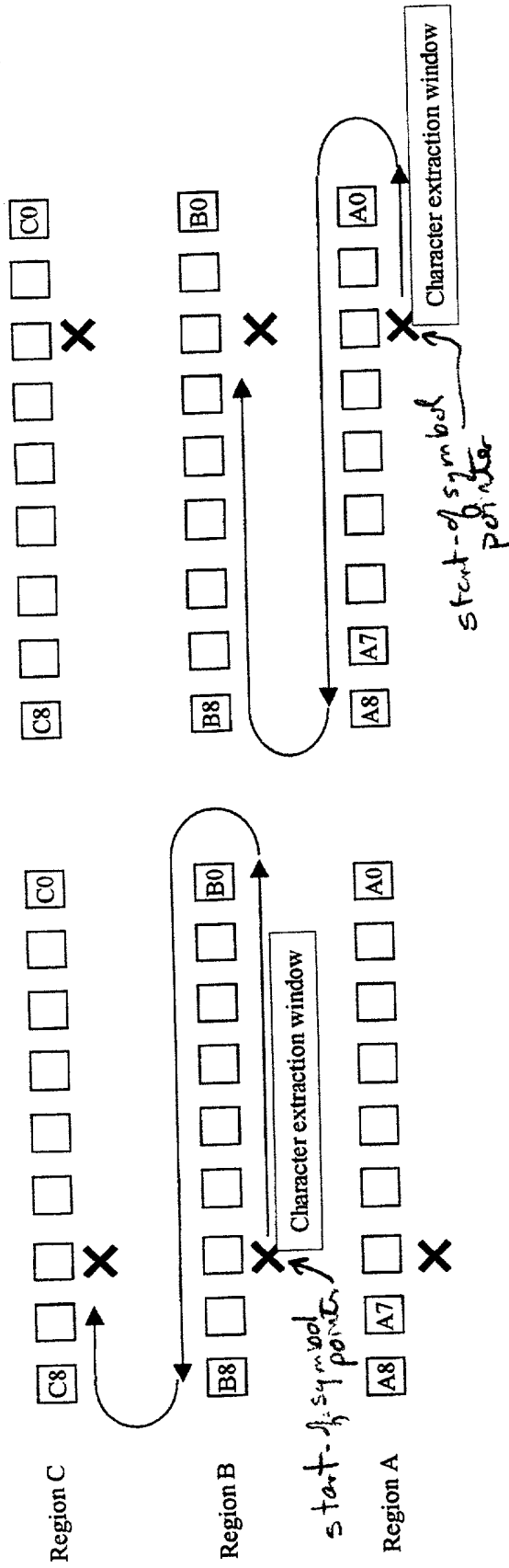


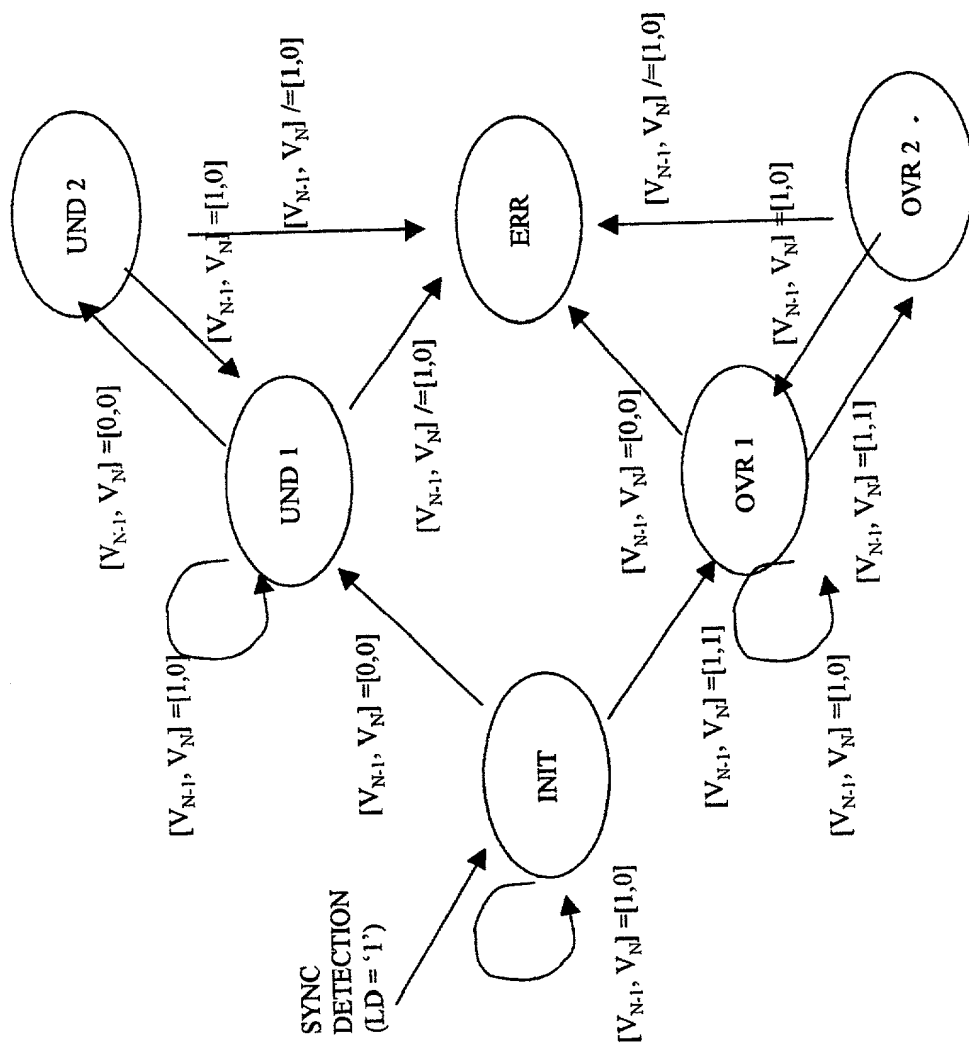
Fig. 43



LD = 1, iHF = 1, iPTR = "000000100"

LD = 1, iHF = 0, iPTR = "001000000"

Fig 44



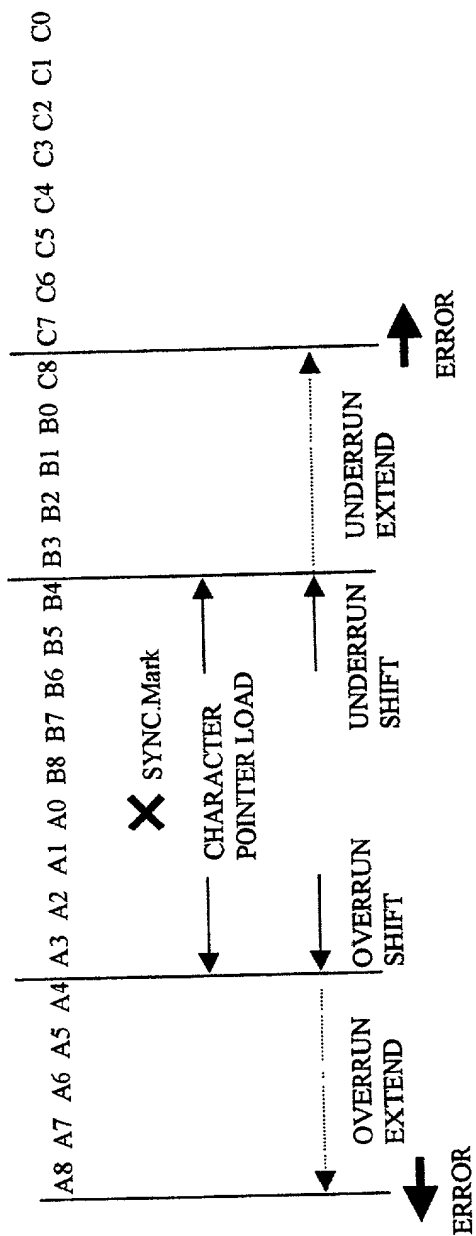


Fig 46

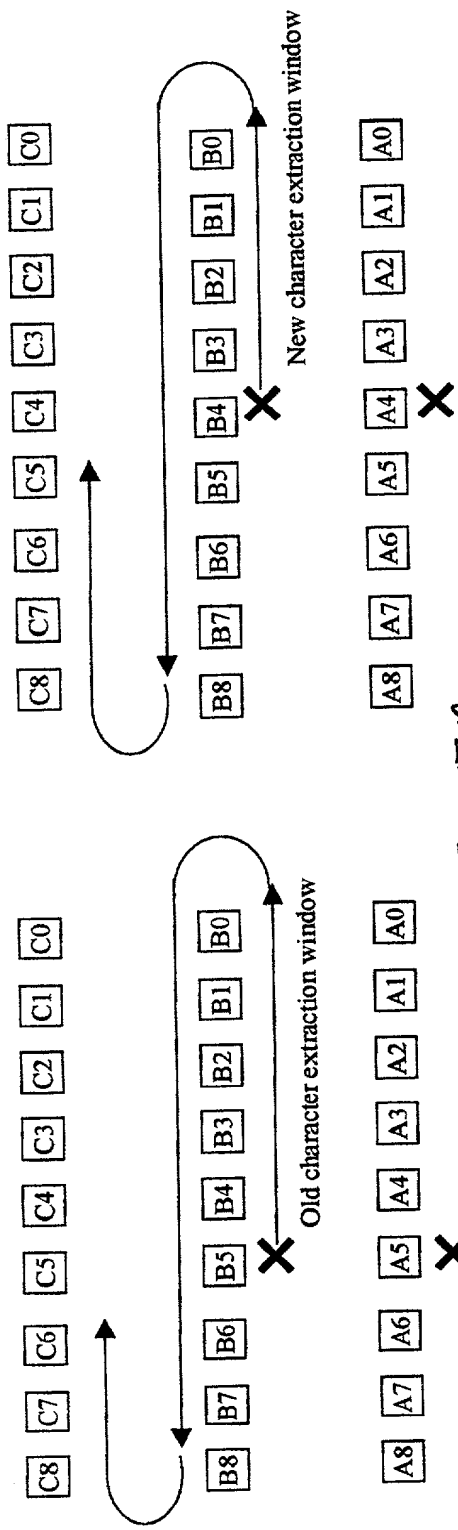


FIG. 47A

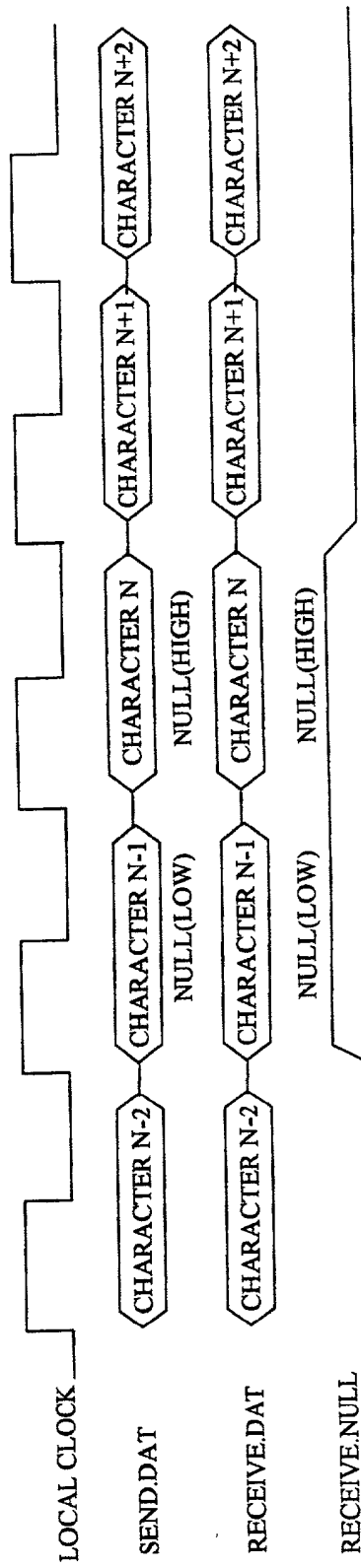


Fig 47B

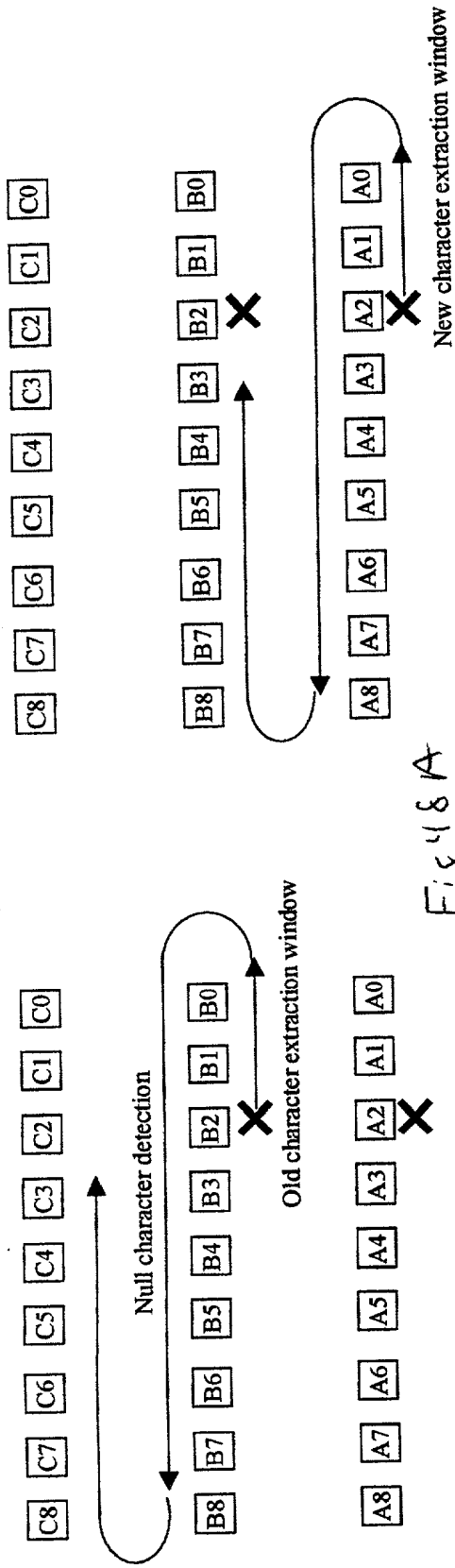


Fig 48A

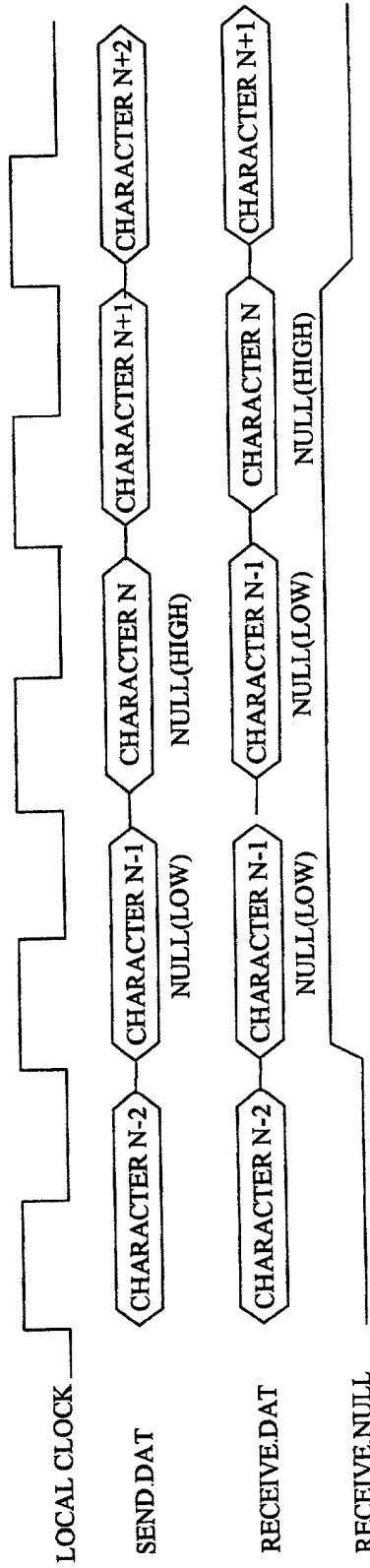


Fig 48B

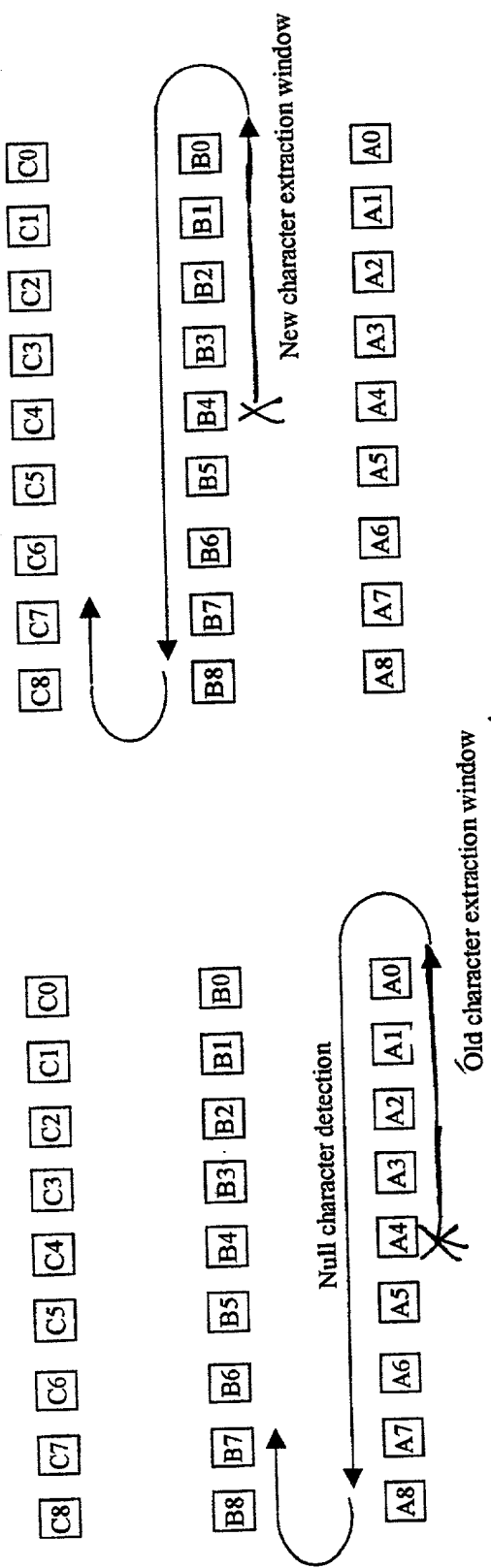


Fig. 49A

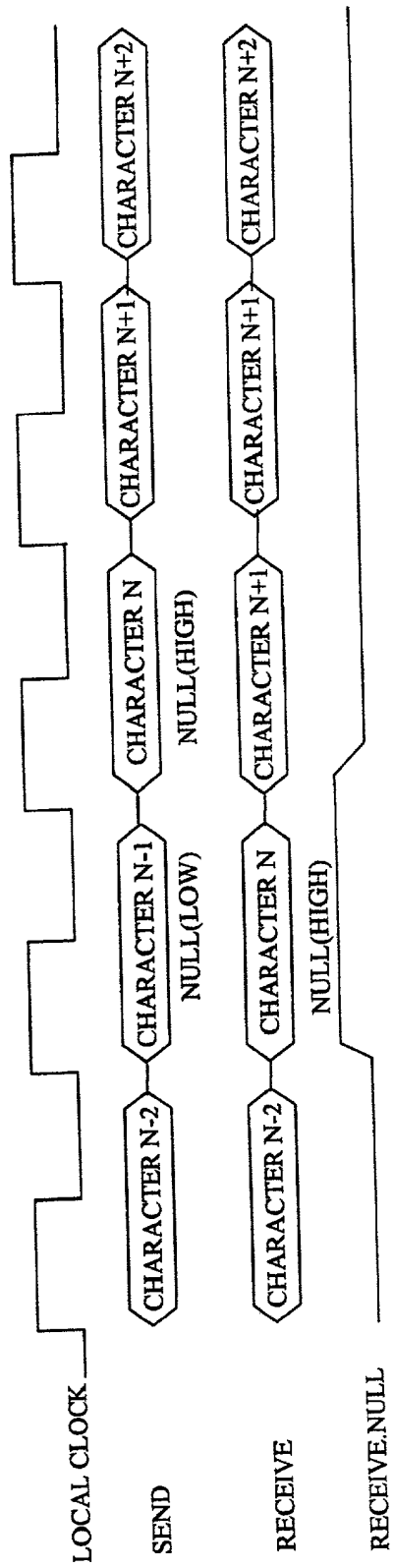


Fig 49B